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advantage is insignificant noise due to bias current (shot noise): noise is dominated by noise voltage and resistor noise.

Note:

For quad and dual op-amps the high, medium and low bias modes are respectively identified by 'no letter', 'M' or 'L' in the device number, e.g. TLC274 is high bias quad, TLC27M2 is a medium bias dual and TLC27L4 is a low bias quad.

Single op-amps (TLC271/251) are programmable by the level of voltage applied to the bias select pin 8. This voltage level has to be $-V_{DD}$ (or single supply GND) to give high bias mode, any voltage in the range $-V_{DD}$ $+0.8V$ and $+V_{DD}$ $-0.8V$ to give medium bias mode and $+V_{DD}$ to give low bias mode.

For further information see section 8 Data Sheets.

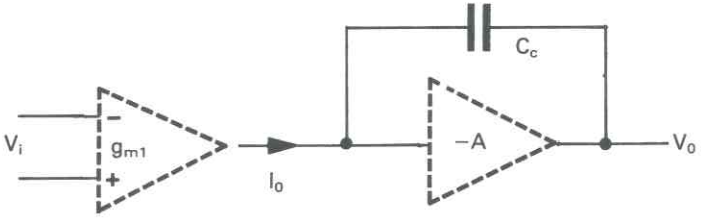
3. LinCMOS Design Characteristics Review

BASIC OP-AMP DESIGN CONSIDERATIONS

This section will give some insight into the basic gain, bandwidth and slew rate characteristics of LinCMOS op-amps in comparison with bipolar types.

A simple conceptual model (Figure 3.1) can be used to describe the internal circuit topology of the classical two stage op-amp. This is essentially an ac model and consists of a differential to single ended converter followed by an inverting amplifier with frequency compensating capacity C_c as shown in Figure 3.1.

Fig. 3.1 Classical two stage op-amp model.



At low frequencies, where the compensation capacity C_c has no effect, the op-amp's overall dc gain can be modelled by two cascaded gain stages. These stages for CMOS are voltage amplifiers with the gain of each stage given by $Av=g_m/g_o$ (g_m=transconductance, g_o=output conductance). For bipolar the first stage is transconductance and the second transresistance giving a voltage gain overall. Where the individual transistor loads reside determines the type of amplifier a stage forms (voltage, transconductance etc.). In CMOS circuits the input impedance of the following stage is so high that the load is only MOS transistor output conductance. In bipolar circuits the low input resistance of the following transistor stages dominate the loads. In general these can be designated R_{L1} and R_{L2} respectively wherever they appear to reside, and for this reason are not shown on Figure 3.1.

Op-amp d.c. voltage gain can be expressed to a first order as:

$$A_{d.c.} = (g_{m1}R_{L1})(g_{m2}R_{L2}) \quad \ldots\ldots \quad (3.1)$$

To give the op-amp overall a.c. voltage gain the differential transconductance stage (Figure 3.1) drives current I_o into the 'virtual earth' node created by the inverting amplifier and the feedback compensating capacitor C_c. This capacitor, with it's associated Miller capacitance at this node, causes the amplifiers of the model to act for a.c. as transadmittance and transimpedance stages respectively. The voltage output is produced by current I_o flowing in C_c with the resulting op-amp a.c. voltage gain:

$$Av = \frac{V_o}{V_i} = \frac{g_{m1}}{I_o} \times \frac{I_o}{\omega C_c} = \frac{g_{m1}}{\omega C_c} \quad \ldots\ldots \quad (3.2)$$

Equating this to 1 gives unity gain-bandwidth or gain-bandwidth product:

$$\omega_1 = \frac{g_{m1}}{C_c} \quad \ldots\ldots \quad (3.3)$$

where ω and ω_1 are frequency in rads/second.

Slew rate is determined by the rate at which capacitor C_c can be charged by current I_o from the first stage and is given by:

$$\text{Slew rate SR} = \frac{dV_o}{dt} = \frac{I_o}{C_c} \quad \ldots\ldots \quad (3.4)$$

substituting for C_c from (3.3)

$$SR = \frac{I_o\omega_1}{g_{m1}} \quad \ldots\ldots \quad (3.5)$$

Circuit time constants for a particular process will determine the frequency compensation (C_c) required in order to keep the circuit stable with a satisfactory phase margin. This is usually specified at a gain of unity and sets the unity gain frequency, ω_1. Other parameters that control the limits on slew rate are from (3.5) g_{m1} and I_o and these have a fixed relationship dependent on process technology. For example in the bipolar process g_m is directly proportional to transistor emitter current

I_e (corresponding to I_o above) and is given by:

$$g_m = \frac{qI_e}{KT} = \frac{I_e}{26mV} \text{ (at 27°C)} \quad \therefore \quad \frac{I_e}{g_m} = \frac{I_o}{g_m} = 26mV$$

and thus for a fixed value of ω_1 the slew rate cannot be improved. It is possible to increase I_o over g_m in the bipolar process by designing the first stage with emitter degeneration (e.g. LM318) but other characteristics may be compromised; in particular V_{IO}, which requires close matching of the emitter resistors, thereby increasing the devices cost.

Using JFET input devices, in the BIFET process, the slew rates attainable are much higher because JFETS have inherently lower g_m for the same bias current. MOS transistors do provide the same slew enhancements as JFETS but greater advantages can be obtained by using a totally MOS (CMOS) structure. MOS transistors have an improved gain performance at low bias currents and process reduced circuit time constants give an inherently higher bandwidth. This reduces the required size of compensation capacitor C_c and allows a higher unity gain bandwidth frequency ω_1. The same performance as general purpose bipolar op-amps is therefore obtained at an order of magnitude less supply current. Additionally higher performance can be obtained by increasing the bias current and therefore performance can be traded against supply current. Figure 3.2 shows the a.c. and d.c. gain performance for the three supply current settings and Table 2.1 allows comparison of the other parameters.

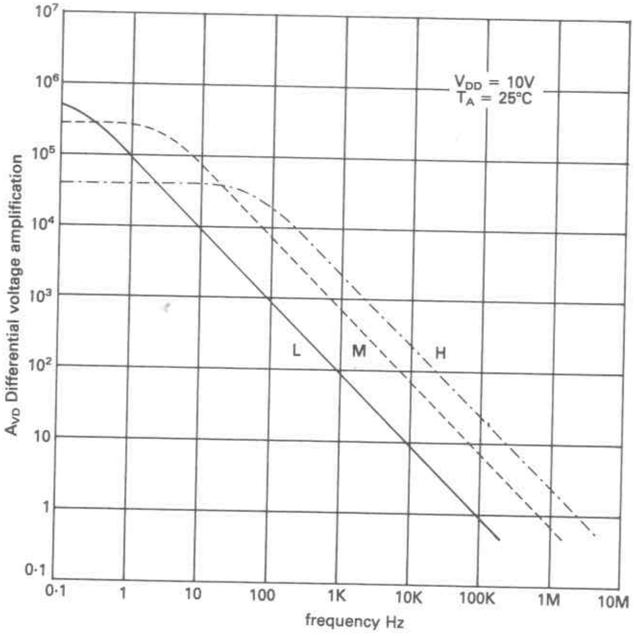
An understanding of how the trade-offs for d.c. and a.c. performance against bias (supply) current occur within the LinCMOS process can be gained by substituting the MOS transistor parameters in the above equations with the following explanation.

For op-amp d.c. voltage gain, $1/g_o = R_L$ is substituted in eqn (3.1) giving:

$$A_{d.c.} = \frac{g_{m1}}{g_{o1}} \times \frac{g_{m2}}{g_{o2}} \quad \ldots\ldots \quad (3.6)$$

An increase in d.c. gain with decrease in bias level is shown by Figure 3.2. With the high and medium bias op-amps the MOS transistor drain current I_D levels give a d.c. voltage gain $A_{d.c.}$ (3.6) that is proportional to $1/I_D$ to a first order. This results because g_m in a MOS transistor is proportional to $\sqrt{I_D}$ and output conductance g_o is proportional to I_D, making the ratio g_m/g_o proportional to $1/\sqrt{I_D}$.

Fig. 3.2 Large-signal differential voltage gain Vs frequency comparison for high (H) medium (M) and low (L) bias modes.



A lower increase in d.c. gain $A_{d.c.}$ (3.6) occurs from medium to low bias levels and tends to a constant value with change in I_D. This results because as drain current I_D decreases to very low levels g_m goes from being proportional to $\sqrt{I_D}$ to being directly proportional to I_D and thus the ratio g_m/g_o tends to a constant value. MOS transistors at these very low I_D levels have a bipolar type g_m and I_o relationship.

For a.c. gain the GBW product equation (3.3) remains true but as the rate of change of g_m is greater between low and medium bias than between medium and high bias, there is a correspondingly greater increase in GBW product. Slew rate is directly proportional to I_D as shown by equation (3.4).

LOW DRIFT VIO

Use of the polysilicon gate process and the careful input circuit design has given the LinCMOS operational amplifiers very good input offset voltage drift characteristics. This is shown in Table 3.1 reproduced from the data sheet. Particularly the 0.1µV/month drift figure shows how stable the process is with time.

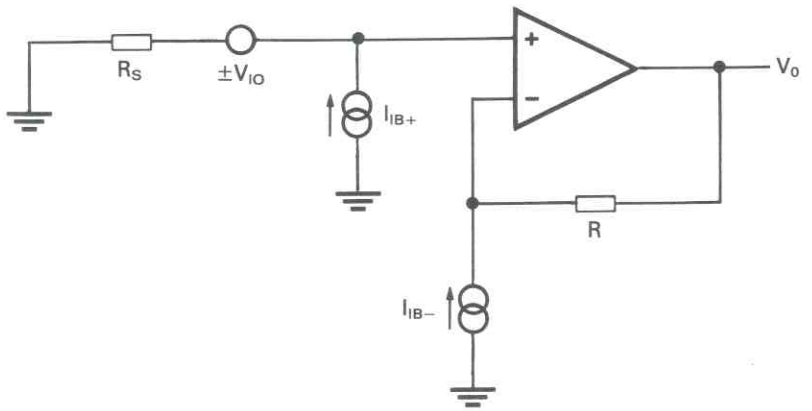
Table 3.1

Parameter Bias	Low	Medium	High
Offset voltage drift (Typ)*	0.1µV/month	0.1µV/month	0.1µV/month
Offset temp coef (Typ)	0.7µV/°C	2µV/°C	5µV/°C

*The data sheet states that these long term drift values apply after the first month. Recent characterisation has shown however that they are equally valid during the first month.

The following shows how the effects of V_{IO} drifts are calculated for the basic inverting and noninverting circuits. Contributors to the output offset are V_{IO}, $I_{IB\pm}$ and I_{IO}, where $I_{IO} = (I_{IB+} - I_{IB-})$.

Fig. 3.3 Non-inverting offset voltage and current model.



$$\text{Output offset } V_o = (I_{IB+})R_s - (I_{IB-})R \pm V_{IO} \quad \ldots\ldots\ldots\ldots \quad (3.7)$$

$$\text{For matched bias resistors } R = R_s,\ V_o = \pm I_{IO}R \pm V_{IO} \quad \ldots\ldots \quad (3.8)$$

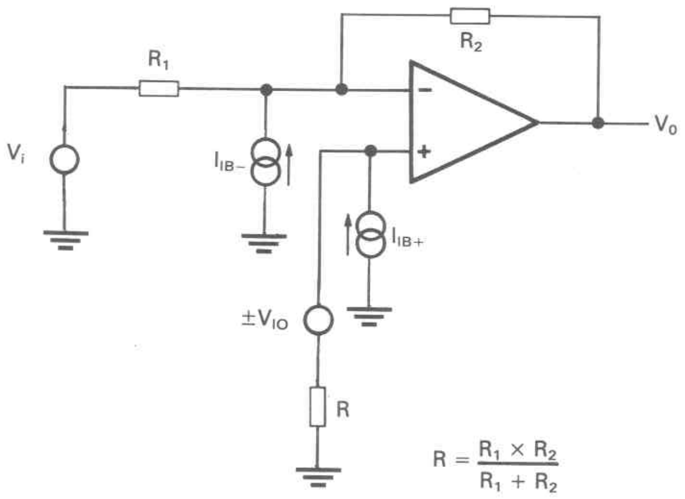
Giving temperature dependance:

$$\frac{dV_o}{dT} = \pm I_{IO}\frac{dR_s}{dT} + R_s\frac{dI_{IO}}{dT} \pm \frac{dV_{IO}}{dT} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.9)$$

For LinCMOS the input offset current has negligible effect except for very high values of feedback and source resistor. R needs to be >10 Mohms to give comparable offset due to I_{IO} as V_{IO}, thus ignoring terms in I_{IO}:

$$dV_o = \frac{dV_{IO}}{dT} \times dT. \qquad dV_{IO}/dT \text{ is called } \propto V_{IO} \text{ in data sheets.}$$

Fig. 3.4 Inverting offset voltage and current model.



For the circuit of Figure 3.4 assuming $V_i = 0$:

$$V_o = \pm V_{IO}\left(1 + \frac{R_2}{R_1}\right) + (I_{IB+})R\left(1 + \frac{R_2}{R_1}\right) - (I_{IB-})R_2 \quad (3.10)$$

For matched bias current resistors i.e. $R = (R_1R_2)/(R_1 + R_2)$

$$V_o = \pm V_{IO}\left(1 + \frac{R_2}{R_1}\right) \pm I_{IO}R_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.11)$$

Giving temperature dependance:

$$\frac{dV_o}{dT} = \left(1 + \frac{R_2}{R_1}\right) \times \frac{dV_{IO}}{dT} \times dT \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.12)$$

assuming R_1 & R_2 are drift free.

Again I_{IO} may be neglected except for very high resistor values (>10 Mohm). This result shows that for an inverting amplifier the gain to input signals V_i is times −1 and to V_{IO} is times 2.

Single operational amplifiers TLC251/271 have provision for input offset adjustment by use of a 25 kohm potentiometer connected between the offset null pins with the wiper connected to $-V_{DD}$ (GND). This adjustment should not be used to compensate for other circuit error voltages. The offset null pins are used to equalise the currents in each half of the input differential amplifier. If these currents are made unequal, to compensate for other error voltages in the circuit, both the temperature and long term specifications will be degraded.

LinCMOS op-amps can be used therefore to produce long term and temperature stable low power amplifiers for interface applications. The effects of input bias current are insignificant and so any temperature dependancy they have will be equally insignificant.

Notes: 1. Very precise circuits need to be concerned with the thermoelectric potentials produced by dissimilar metals such as the copper and tin/lead solder (1 to 3μV/degC) circuit connections.

2. Matching input resistances to equalise the d.c. input offset due to the bias current will not give the best a.c. noise performance. At the levels of source and feedback resistance that give resistor noise levels

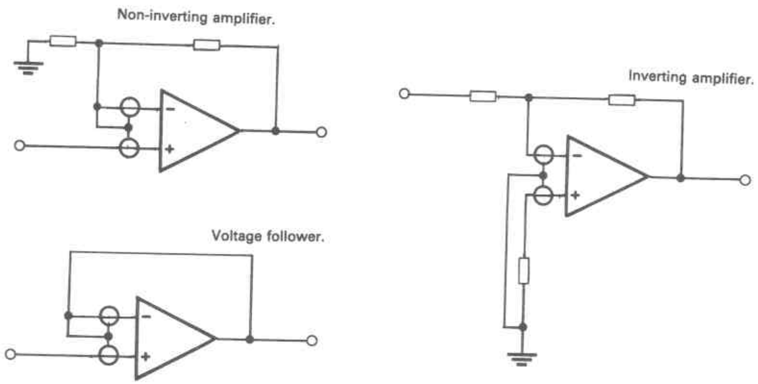
comparable with voltage input noise (e_n), the d.c. offsets due to bias current compared with V_{IO} will be small. Thus input resistors matching should not be included for best a.c. noise performance (see noise section).

LOW INPUT BIAS AND OFFSET CURRENT

PMOS input transistors have very high input impedance and potentially non-existent input currents. Practice dictates the inclusion of ESD protection circuits which still give LinCMOS op-amps an order of magnitude less bias current than BIFETs over temperature (see Table 2.1). For the above non-inverting stage a source resistor R_s of 10Mohms still only gives an offset due to I_{IO} (300 pA) equal to V_{IO} (3mV). If offset is not an important parameter much higher resistor values can be used if this is within a.c. noise constraints.

Use of high value feedback resistors has several advantages: it takes full use of the low-power capabilities, it allows the use of smaller lower cost and more precise capacitors in filter and timing circuits and it reduces the loading on the output stage allowing a wider output voltage swing.

Fig. 3.5 Guard ring schemes.



However there are precautions that have to be observed with the use of high value feedback resistors:

Leakage currents on printed circuit boards can cause problems. It is good practice to include guard rings around inputs in the form of a track on the PCB that encloses the input pins. These should be driven from a low impedance source at the same voltage as the inputs, Figure 3.5 shows three common schemes.

The input capacity of the device and strays can cause feedback poles and excess phase shift and thus stability problems. These effects can be minimised by keeping the feedback resistor connections as close as possible to the input pins and by the use of small value feedback capacitors (see stability section).

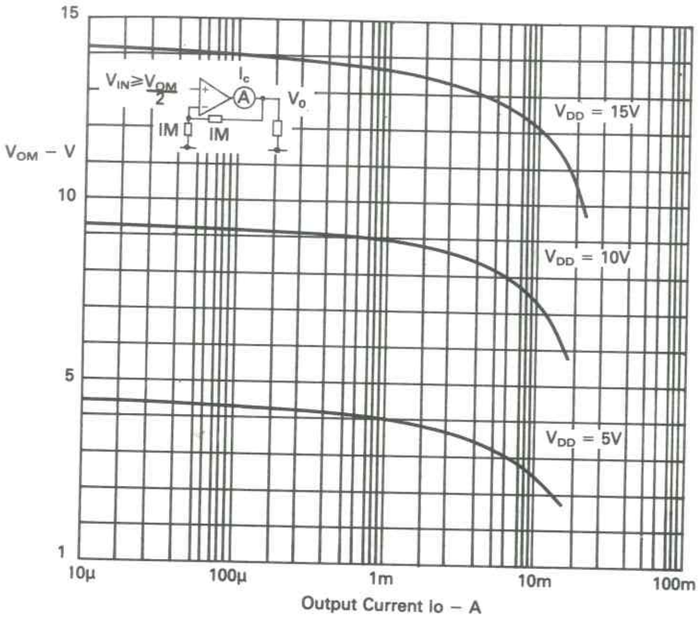
OUTPUT DRIVE CAPABILITY

From the schematic diagram (Figure 2.3) of the LinCMOS op-amp it can be seen that the output circuit is comprised of NMOS transistors N_4, N_5 and current limiting resistor R_3. For very light output loads transistor N_4 provides bias current for N_5 to allow linear operation.

Although the LinCMOS op-amp will operate with +/− supply rails it's output stage has been optimised for single rail applications. With a load connected between the output and 0V transistor N_5 supplies the output current and N_4 pulls the output down to within a few millivolts of 0V. The voltage output swing V_{OM} extends from the supply voltage V_{DD} less N_5's V_{GS} and P_4's V_{DS} to 0V. The magnitude of N_5's V_{GS} depends on the backgate voltage between the backgate of N_5 (which is the substrate) and the source of N_5, the output. As the output voltage increases above the substrate, the V_{GS} of N_5 increases. However this still results in a V_{OM} that is a higher percent of V_{DD} for higher supply voltages V_{DD}. Typical values of V_{OM} versus output current are plotted for three values of supply voltage V_{DD} 5V, 10V and 15V in Figure 3.6.

Where greater V_{OM} is needed, such as when interfacing to A–D converters operating on 5V supplies or supplying higher output currents, it can be achieved with a pull-up circuit. The simplest of these is a resistive pull-up the value of which can be calculated as shown in Figure 3.7 and equation (3.13).

Fig. 3.6 Maximum output voltage V_{OM} Vs. output current I_0 with V_{DD} as parameter.



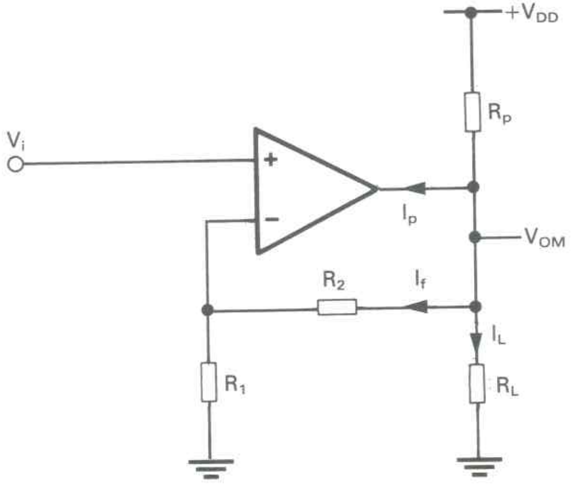
$$Rp = \frac{V_{DD} - V_{OM}}{I_f + I_L + I_p} \quad \text{. . . . .} \quad (3.13)$$

Where I_p is the pull-up current required by the op-amp, and is typically 0.5μA.

For example at V_{DD} = 5V and a required V_{OM} = 4.8V

	$R_1 = R_2$ ohms	R_L ohms	Needed R_p ohms	Sink I_o mA. due to R_p.	V_o offset from GND
(a)	1M	100k	3.9k	1.28	approx 100mV
(b)	100k	10k	390	12.8	approx 1V

Fig. 3.7 Resistive pull-up R_p.

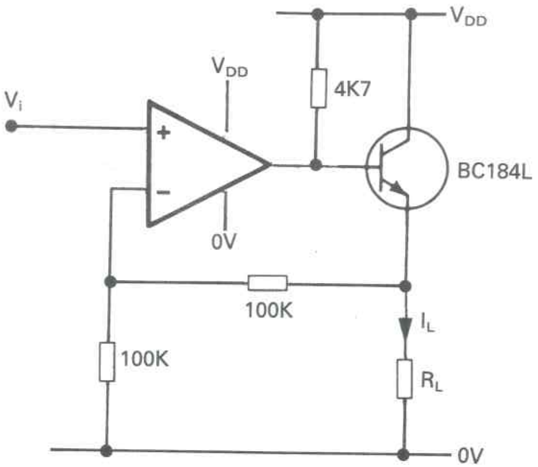


There are two disadvantages to using a simple resistive pull-up. Firstly pull-down transistor N_4 has to sink a comparatively large current. N_4 behaves like a linear resistor in this situation with an on resistance between 60–180 ohms depending on how hard the input to the op-amp is driven. With very low values of pull-up resistor a voltage offset from 0V at the output will occur. Secondly the pull-up resistor acts as a drain load to transistor N_4 and the gain of the op-amp is reduced at Vout levels where N_5 is not supplying the output current. A load of 1kohm will reduce the gain of the op-amp to approximately 3500. This effect is also observed when in dual supply operation using low load values on negative output swings.

An improved pull-up can use an emitter follower to supply a larger load current and bring the V_{OM} to within approximately 0.8 volts of the positive supply. Figure 3.8 shows a circuit for single rail application.

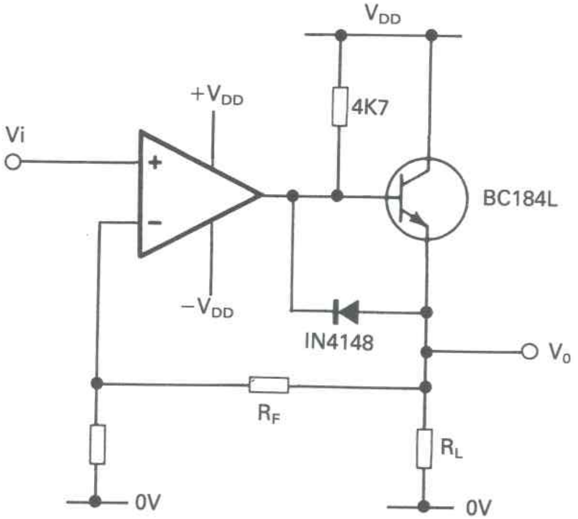
Figure 3.9 shows a circuit suitable for –/+ supply rails d.c. and low frequency applications. The speed at which the circuit will operate is dependent upon the rate the op-amp output voltage will slew across the transistor and diode offset voltages.

Fig. 3.8 Single rail load current boost circuit.



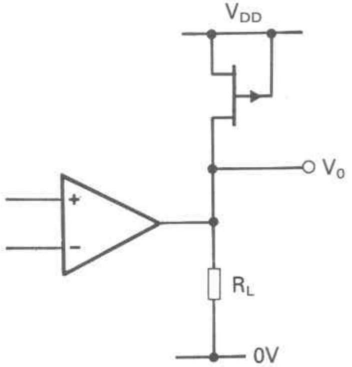
typ I_L = 20mA @ 4V output
= 5mA @ 4.2V output

Fig. 3.9 ± supply load current boost circuit.



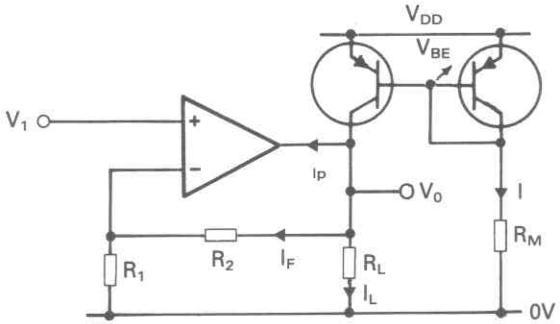
Another alternative is to use a p-channel depletion mode FET as a current source as shown in Figure 3.10. Optimally the FET chosen would supply only the load, feedback and pull-up currents at the highest operating V_{OM} and saturate at that value so that the pull-down offset is minimised.

Fig. 3.10 P channel FET pull-up.



A more successful pull-up circuit which allows the pull-up current to be defined at the optimal value employs two pnp transistors in a current mirror configuration as shown in Figure 3.11.

Fig. 3.11 Current mirror pull-up.



Thus $$I = \frac{V_{DD} - V_{be}}{R_m} = I_p + I_f + I_L \ldots\ldots\ldots\ldots \quad (3.14)$$

For $V_{DD} = 5V$, required $V_{OM} = 4.8V$, $R_1 = R_2 = 100k$ & $R_L = 10k$ then $R_m = 8.2k$.

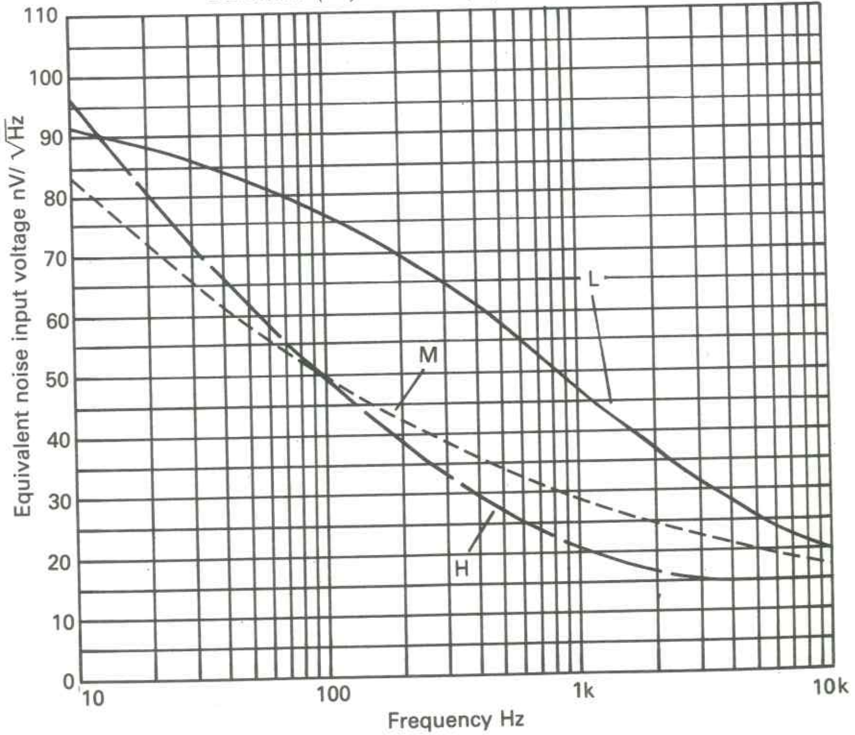
LinCMOS NOISE PERFORMANCE

Introduction

Noise performance of a system is determined by the first stages in the circuit. For an audio or video system where human perception uses the signal to mask the noise this is usually expressed in terms of signal to noise ratio or noise figure. For an analogue to digital conversion process noise determines the ultimate resolution achievable and should generally be less than the least significant bit (LSB). (There are digital filtering techniques that use noise to improve system performance by reduction of quantisation error.) The lower limit to dynamic range is set by the noise floor in any system, this includes analogue circuit noise and, in any analogue to digital conversion, the quantisation noise.

The LinCMOS op-amp typical noise voltage performance for the three supply current versions is shown in Figure 3.12.

Fig. 3.12 Equivalent input noise Vs. frequency for High (H), Medium (M) & Low (L) bias modes.

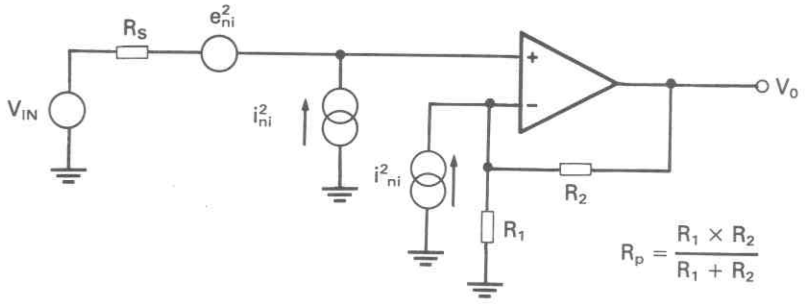


Low input bias currents of the PMOS input transistors give a very low noise current which is usually insignificant and need not be considered. This is shown to greatest advantage when using higher values of circuit impedances (greater than 50kohms). Bipolar op-amps have higher bias and noise currents which dominate the noise performance as circuit resistances are increased. It will be seen below that much higher resistor values can be used compared with bipolar for a similar noise performance which is then dominated by resistor noise.

Noise Design Steps

Initially all noise sources have to be identified and an estimation made of whether each source is significant to noise calculations. See the equivalent circuit Figure 3.13 for a non-inverting op-amp. As the noise signals in the equivalent circuit appear at the non-inverting input noise gain is always that of a non-inverting amplifier. Signal gain is dependent on where the signal is applied. RMS addition is used with uncorrelated noise sources and any noise that is less than 1/2 of the largest noise will result in less than 12% error i.e. $\sqrt{1 + 0.5^2} = 1.12$.

Fig. 3.13 Noise model.



where e^2_{ni} & i^2_{ni} are the op-amp mean-square noise sources.

The noise sources are:

(i) The equivalent op-amp noise voltage source e_{ni} in V/$\sqrt{Hz}$

(ii) Johnson noise due to source (R_s)

and feedback resistors (R_p): $e_{nR} = \sqrt{4KTRB}$ . . . . (3.15)

where K = 1.38×10^{-23} Boltzmans constant in Joules

T = 298°K (25°C)

B = Bandwidth

R = effective resistance.

Giving $e_{nR} = 0.1283\text{nV} \times \sqrt{R}/\sqrt{Hz}$. . . . . (3.16)

(iii) Shot noise due to input bias current:

$i_{ni} = \sqrt{2qI_BB}$ Amps/$\sqrt{Hz}$ . . . . (3.17)

($q = 1.6 \times 10^{-19}$ coulombs)

Hence the total noise referred to the non-inverting input is:

$e_{ntot} = [e_{ni}{}^2 + e_{nRs}{}^2 + e_{nRp}{}^2 + i_{ni}{}^2\,(R_s{}^2 + R_p{}^2)]^{1/2}$ . . . . (3.18)

where $R_p = \dfrac{R_1R_2}{R_1 + R_2}$

For example if $R_s = R_1 = R_2$ = 100kohms in the above circuit the equivalent noise voltage from each source is:

e_{ni} = 38nV/$\sqrt{Hz}$ for the Medium bias LinCMOS op-amp @ 1kHz.

e_{nRp} = 28.7nV/$\sqrt{Hz}$ and e_{nRs} = 40nV/$\sqrt{Hz}$

$[i_{ni}{}^2\,(R_p{}^2 + R_s{}^2)]^{1/2}$ = 1.5nV/$\sqrt{Hz}$ calculated using an input noise current of 13.86 fA/$\sqrt{Hz}$ (from a bias current of 600pA). This value of noise voltage is insignificant when compared with e_{ni} and e_{nRs}. The total noise equivalent voltage at the input is 62nV/$\sqrt{Hz}$.

Using the same resistor values in a circuit employing the 741 with typical $e_{ni} = 22nV/\sqrt{Hz}$ and $i_{ni} = 0.55pA/\sqrt{Hz}$ the equivalent noise voltage due noise current is $61.5nV/\sqrt{Hz}$. This level of noise current makes a significant contribution and gives a total noise voltage of $82nV/\sqrt{Hz}$.

For comparison if the resistor values above are increased to 1Mohm then the following results are obtained:

$$e_{nRp} = 90nV/\sqrt{Hz} \text{ and } e_{nRs} = 128nV/\sqrt{Hz}$$

Equivalent noise voltage due to input current becomes $15.5nV/\sqrt{Hz}$ for LinCMOS and $615nV/\sqrt{Hz}$ for the μA741.

This illustrates that, for LinCMOS, noise due to noise current is insignificant but is instead dominated by input noise voltage e_{ni} and source resistance. For the bipolar device however, the noise current is dominant.

In practice both amplifier transfer functions and noise spectral density are functions of frequency. These transfer functions include the finite bandwidth and skirt response of filters and equalisers. The noise spectral density includes flicker (1/f) with the flat thermal noise. These effects necessitate determining the equivalent "brickwall" noise bandwidth from the transfer function and then making a summation of the mean square noise voltage over this bandwidth.

The noise bandwidth is called the Noise Equivalent Bandwidth (N.E.B.) and is derived by considering the rms noise from an amplifier of gain A with transfer function H(f) and total mean square noise e_{ntot}^2 as follows:

$$Vn = \left[\int_0^{\alpha} e_{ntot}^2 \times A^2 \times |H(f)|^2 \times df\right]^{1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \text{(3.19)}$$

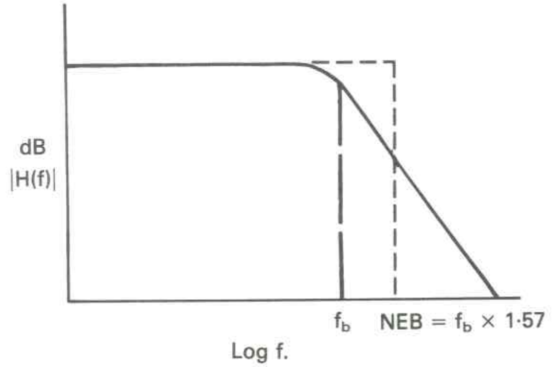
assuming constant spectral density for e_{ntot}^2

$$Vn = e_{ntot} \times A \times \left[\int_0^{\alpha} |H(f)|^2 \times df\right]^{1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \text{(3.20)}$$

$$N.E.B. = \int_0^{\alpha} |H(f)|^2 \times df \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(3.21)}$$

This is shown in Figure 3.14 for a 1 pole filter with break frequency f_b whose N.E.B. is $f_b \times 1.57$ (π/2)Hz.

Fig. 3.14 Noise equivalent bandwidth.



In simple cases the N.E.B. of a transfer function or circuit impedance may be evaluated algebraically but in more complicated cases it is best evaluated numerically with the aid of a numerical integration routine.

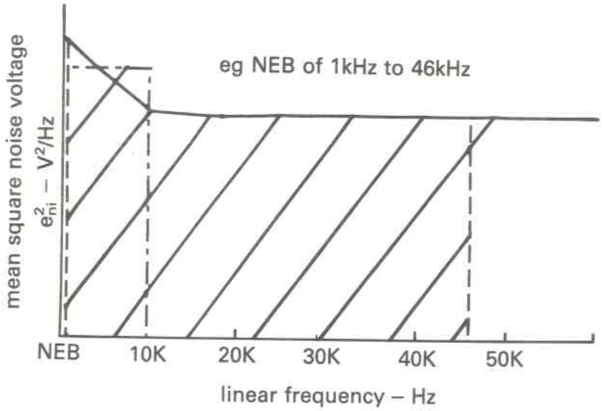
Thus the rms noise output of an amplifier is:

$$Vn = \sqrt{e_{ntot}^2(f)} \times \sqrt{N.E.B.} \times A \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(3.22)}$$

where $A = 1 + \frac{R_2}{R_1}$ for both inverting and non-inverting configurations as the noise appears directly as an input to the non-inverting input of the op-amp.

A graphical method can be used to include the frequency dependent effects of noise spectral density. The first step is to make a sum at decade or less frequency intervals of the mean square voltage/Hz contribution of each noise source. Then a straight line graph of mean square noise voltage/Hz versus frequency is plotted on linear scales. The mean square noise voltage over the N.E.B. is calculated by a summation of the values of mean trapezoidal heights times the corresponding base line. Figure 3.15 shows an example.

Fig. 3.15 Mean square noise summation example.



STABILITY

Stability of a negative feedback amplifier is dependent on the loop phase shift and gain characteristics. That is, the gain and phase shift of the amplifier and feedback network in cascade. This is commonly expressed as phase margin and is the amount by which the excess phase shift due to the amplifier and feedback network is less than 180° when the loop gain is unity. Excess phase shift is the additional phase shift in the loop over the 180° due to negative feedback.

Bode plots of open loop gain, on a log (dB) scale, and phase shift versus log frequency are plotted on data sheets and are typically shown in Figure 3.16 for the LinCMOS TLC271 (high bias). By plotting the closed loop gain on the Bode plot, as shown, the frequency where loop gain ($A_{OL}\beta$) equals unity gives the operating phase margin on the corresponding phase shift plot. Thus in general phase margin can be determined for any value of closed loop gain at loop gain equal to unity. Phase margin is quoted in data sheets at the worst case which is when closed loop gain is unity (voltage follower configuration). Although the gain versus frequency Bode plot does not show higher order frequency roll off effects, these are indicated on the phase shift plots as small contributions to the excess phase. Using these plots and the standard equations shown for a feedback amplifiers much can be understood about an op-amps a.c. performance.

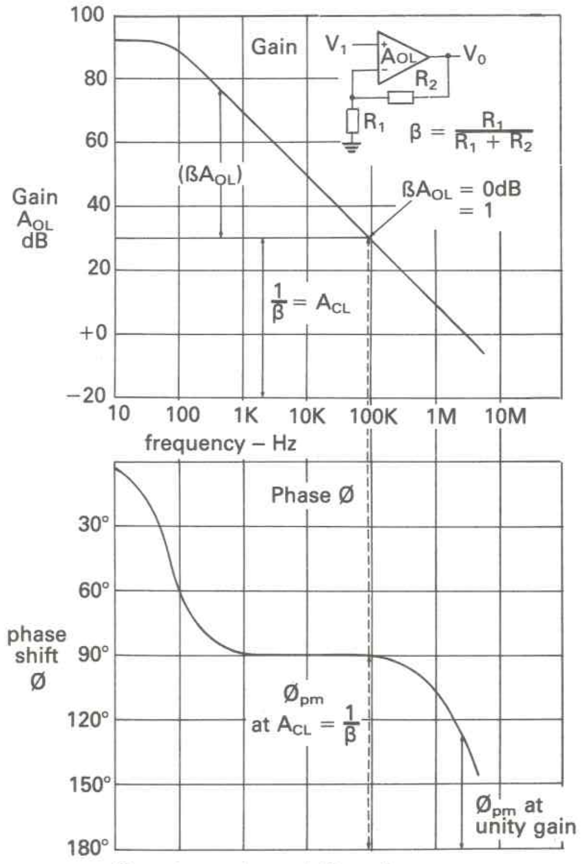
$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} \quad \text{.......} \quad (3.22)$$

Expressed in dB's. For $A_{OL} >> 1$ where $A_{CL} = 1/\beta$

loop gain = open loop gain − closed loop gain

$$A_{OL}\beta = A_{OL} - 1/\beta \quad \text{.......} \quad (3.23)$$

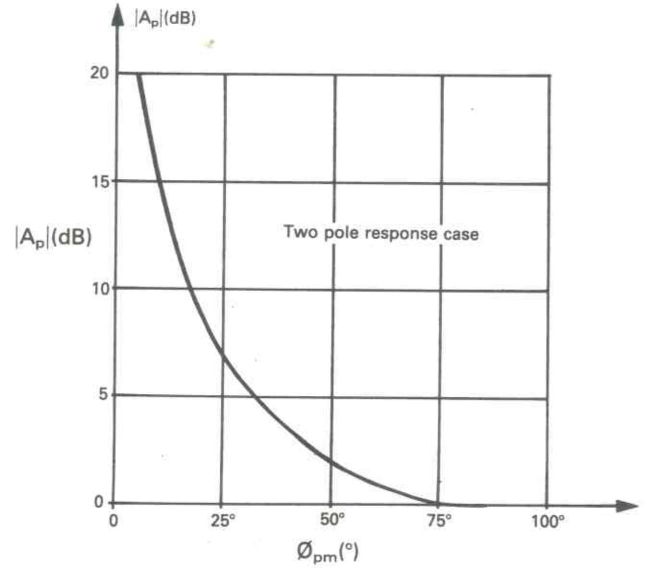
Fig. 3.16 Open loop gain A_{OL} and phase shift Ø Vs. frequency (TLC271 'H').



Open loop phase shift vs. frequency.

A typical response of an op-amp internally compensated for unity gain operation is shown in Figure 3.16. Op-amps of this type have one break frequency (pole) positioned at a low frequency to dominate the phase response versus frequency to ensure stability at unity gain with an acceptable phase margin. The total excess phase at unity gain will be the 90° due to the compensation pole plus additional phase shift from other high frequency poles within the op-amp. Total loop ($A_{OL}\beta$) excess phase shift of less than 180° but more than 90° will cause some peaking of the closed loop gain response at the bandwidth limit. Associated with this will be overshoot and ringing in the transient response. Figure 3.17 shows a graph of gain peaking versus phase margin and Figure 3.18 shows transient response.

Fig. 3.17 Gain peaking Vs. phase margin $\varnothing_{pm}$.



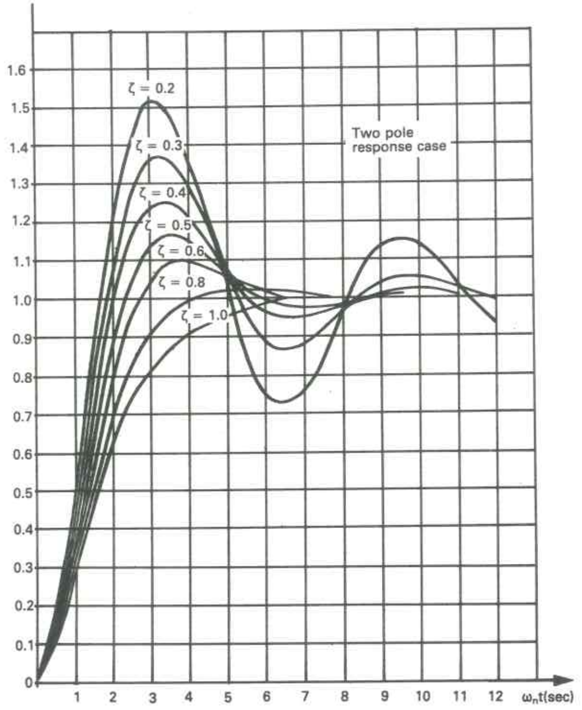
Feedback poles

A feedback pole exists at the input of all op-amps due to the input (5pF typ) and stray capacity with the parallel combination of the feedback resistors, see Figure 3.19.

$$f_c = \frac{1}{2\pi C s R_1 // R_2} \tag{3.24}$$

Fig. 3.18 Transient response Vs. damping factor.

$$\zeta = \frac{1}{\sqrt{\frac{\cos \varnothing_{pm}}{\sin^2 \varnothing_{pm}}}}$$ gives relationship between phase margin $\varnothing_{pm}$ & ζ



$$\phi = \tan^{-1}\left(\frac{f}{f_c}\right) \tag{3.25}$$

There is more likelihood of the feedback pole making a significant contribution to excess phase shift, and thus causing instability, using low power circuits with high values of feedback resistors (100k's) than with the more usual 10k's of bipolar op-amps. The phase contribution can be calculated from equation (3.25) above using the cut off frequency from (3.24), f is the frequency where the loop gain is unity. Values for f/fc = 6 are 10° and f/fc = 10 are 5.7°.

Practical solutions to this problem are to minimise the stray capacitance by making the resistor connections physically close to the IC pins and, where necessary, add a feedback capacitor C_f as shown in Figure 3.19. The value of C_f should be $\leq (R_2C_s)/R_1$ Larger values of C_f can be used to improve the phase margin and reduce gain peaking. This also reduces the bandwidth which can be useful in reducing noise.

Fig. 3.19 Feedback pole compensation capacity C_f.

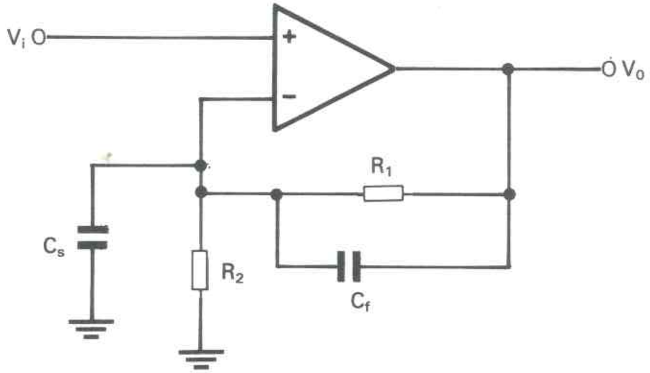
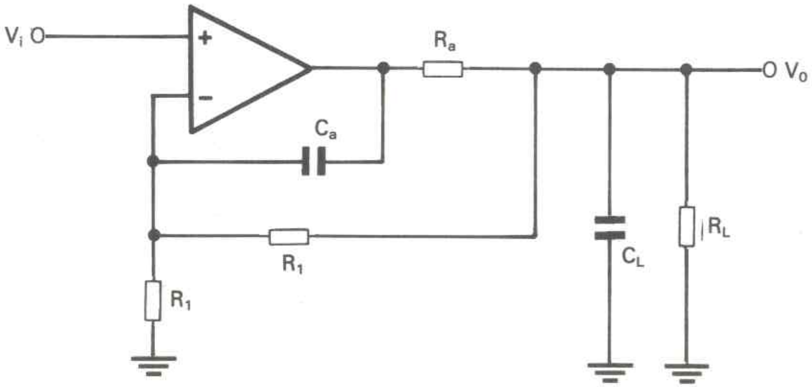


Fig. 3.20 Output pole compensation capacitor C_a and resistor R_a.



Output poles

A pole exists at the output of an op-amp as a result of the op-amp's output resistance and the load capacitance and can be a cause of instability due to the excess phase introduced. One source of load capacity are cables, which are entirely capacitive for lengths much shorter than a wavelength. The LinCMOS devices are specified with 100pF load capacitance. The above equations allow the calculation of the excess phase contribution as for the feedback pole. A circuit solution to the problem of high capacitive loads is shown in Figure 3.20. The values for R_a and C_a are best determined empirically.

The above description has outlined the way op-amp stability is specified in terms of phase margin and how the concept of excess phase round a feedback loop can be used to understand stability problems. This has been concerned only with circuit constraints and has assumed perfect physical circuit layout and decoupling. However stability problems are often encountered because of insufficient or incorrect decoupling, or because the connection of components to ground is in the wrong order. When designing analogue circuits there is no substitute for a thorough understanding of where circuit currents flow. From this understanding decoupling can be provided to aid current flow in the correct path and thereby prevent instability. Also ground connections should be made to prevent load currents flowing in small signal input circuits, causing instability or more subtly a performance degradation in the form of d.c. errors or a.c. distortion.

Care should be exercised in the value and type of capacitors chosen for decoupling. Wiring at the higher frequency end of an op-amp's range can present enough inductance to resonate with small value decoupling capacitors. This is cured by larger values or by inclusion of small values of series resistor. The message is that the perfect (infinite sink) ground does not exist and the unthoughtful use of decoupling capacitors can cause more problems than they solve.

ELECTROSTATIC DISCHARGE PROTECTION

All semiconductor devices, MOS and Bipolar, are susceptible to electrostatic discharge (ESD) at some level: most are ESD sensitive at 2kV or less. Greater attention has been paid to this subject with the introduction of MOS memories and CMOS logic, and LinCMOS shares in the development work that has taken place to reduce the sensitivity of these devices to ESD. Improvements in ESD thresholds are continuously being made in all these product areas but these will not be able to achieve the sort of levels that can be encountered in uncontrolled and careless handling of devices. To ensure the performance of devices is maintained, good handling and packaging practices should always be observed. (Contact T.I. Customer Response Centre for further information.)

CMOS devices are voltage sensitive due to the basic input structure consisting of a dielectric between two conductive layers that can be destroyed by an electric field of about 60V. This dielectric is protected by an input circuit which consists of diodes, zeners, resistors and thickfield MOS transistors. Outputs also need to be protected and this is achieved using small value resistors and thickfield MOS transistors.

The protection circuits cause the input bias currents to be temperature dependent and have the characteristic of a reversed bias diode within the values quoted in the data sheet.

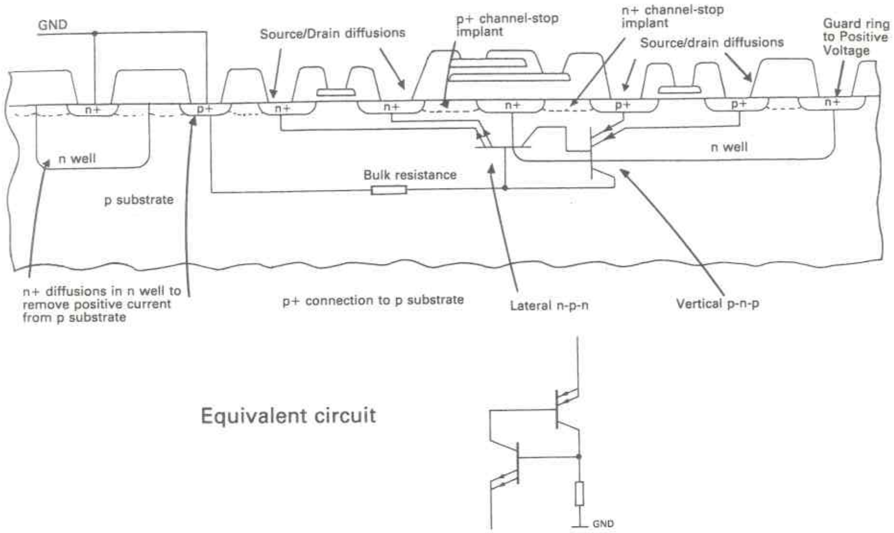
These circuits will prevent catastrophic failure when tested with voltages up to 2kV according to MIL STD 883B method 3015.1. This test specifies 5 discharges at one second intervals of a 100pF capacitor at 2kV through a 1.5kohm resistor into each terminal. The data sheet warning of parametric degradation after such a test substantially refers to an increase of input bias current I_{IB} to low tens of nano-amps.

LATCH-UP

Latch-up is the uncontrolled flow of current through the parasitic thyristors inherent in all CMOS devices (see Fig. 3.21). The current path is generally between the V_{DD} and ground pins of the IC and can be triggered by excessive currents in the signal pins or by di/dt stress of the V_{DD} pin. Once the thyristor is triggered, the current flow is limited only by the impedance of the power supply and the forward resistance of

these thyristors. This can result in the destruction of the device. Latch-up is more likely to occur at high supply voltages and temperatures.

Fig. 3.21 Latch-up mechanism, & prevention.



Conditions permitting latch-up exist whenever the gain product of the parasitic n-p-n and p-n-p transistors forming the thyristor exceeds unity. In the LinCMOS N−well process a vertical p-n-p is formed by the P+source/drain, N− well and P− substrate and a lateral n-p-n is formed by the N+source/drain, P− substrate and N− well. This N−well configuration gives the minimum gain for these transistors. The parasitic thyristor is triggered by bulk currents in the substrate.

To minimise the chance of latch-up, extra diffusions regions are introduced which shunt current out of the substrate and away from the bases of the parasitic transistors. This is achieved in LinCMOS by the use of N+ guard rings around all N−well edges with P+ guard rings around particularly sensitive structures. The LinCMOS devices are tested to ensure latch-up does not occur with −100mA drawn from any pin with normal supply voltages.

Application circuits should be designed to prevent latch-up inducing currents being injected into the substrate. ESD protection diodes should not by design be forward biased. This is achieved by not allowing input and output voltages to go more than 0.3V beyond either supply rail. For this reason care should be used when capacitively coupling pulse generators and using capacitors in pulse circuits. Supply transients should be prevented by good decoupling practice; that is by making sure there are no common impedance earth paths with other circuits and by having a decoupling capacitor close to the V_{DD} and ground pins. Proper sequencing of supply voltage and input signals should be observed to prevent parasitic diodes being biased on and inducing latch-up. The supply voltage should be established before the input signal voltages. This is true for any junction isolated integrated circuit process whether bipolar, BIFET or CMOS.

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4. Applications Section

INTRODUCTION

This section contains some application examples for op-amps with particular reference to the LinCMOS TLC27__/25__ range. No claim is made for the circuits' originality but rather they appear as an aid to memory. Most have some circuit analysis to illuminate operation and stimulate further user ideas.

As described in the previous section, the LinCMOS op-amp's low input bias performance eliminates the need for bias compensation resistors thus simplifying circuits. Most circuits indicate how they should be biased for single supply operation to take advantage of the common mode range to GND ($-V_{DD}$) performance. This is indicated by a V_b rail which for single rail operation is a bias voltage and for +/− supply rails the usual GND (0V). Bias voltage can be most often derived by using a simple resistive divider, but to provide a low impedance source 'spare' op-amps in quads, for instance, can be utilised.

The trade-off between power and op-amp speed (gain-bandwidth product and slew rate) by selection of supply current through bias mode (H, M or L) has been described above. When making the bias mode selection careful evaluation of the bandwidth and slew rate requirements of the signal being conditioned should be made.

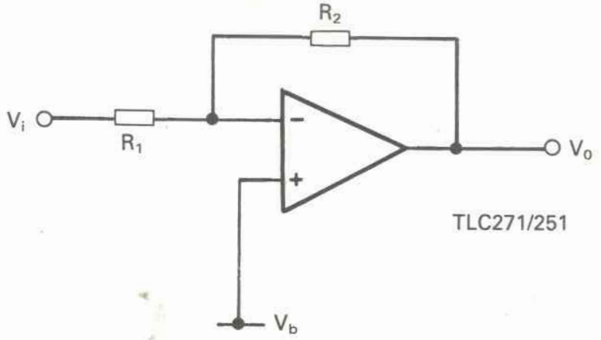
Enough bandwidth should be available so that the open loop gain exceeds the closed loop gain by a sufficient amount (i.e. 10×) at the frequencies of interest to give the required gain error or distortion performance. For specialised applications such as filters the bandwidth, and consequently the phase response, has an impact on the filters' accuracy (and sometimes stability).

Slew rate requirements are determined by the rate of change of output voltage with time given by the maximum value of $d(V_O(t)/dt$, where $V_O(t)$ is the output voltage function with time. For sinewaves ($V_{opk}.\sin\omega t$) the maximum slew rate is $\omega.V_{opk}$, and thus both frequency and signal amplitude are important. For complex feedback networks (such as filters) instability at varying output amplitude levels can be caused due to phase shifts at the onset of slew rate limiting.

AMPLIFIERS

Basic Inverting

Fig. 4.1 Basic inverting amplifier.



The expression for output voltage is given below including a bias or level shift voltage V_b which is necessary for single rail operation. The gain error term $[1 - 1/A\beta]$ is included in the equation, for very large A this tends to unity.

$$V_o = -\frac{R_2}{R_1}\left(1 - \frac{1}{A\beta}\right) V_i + V_b \quad \text{where } \beta = \frac{R_1}{R_2 + R_1}$$

hence the gain for operation around the bias level is:

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

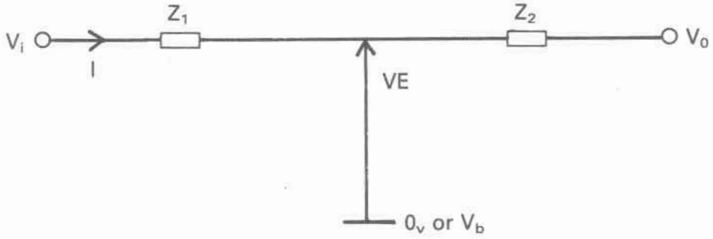
The 'virtual earth' that appears at the inverting input of the op-amp is a useful concept when calculating transfer functions thus:

For V_e referred to 0V in general $V_i = IZ_1$ & $V_o = -IZ_2$ giving

$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$

For V_e referred to V_b: $V_i - V_b = IZ_1$ & $V_o - V_b = -IZ_2$ giving

Fig. 4.2 Virtual earth diagram.



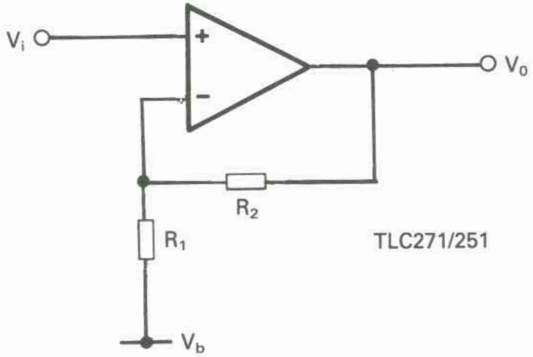
$$V_o = -\frac{Z_2}{Z_1} V_i + V_b \left(1 + \frac{R_2}{R_1}\right)$$

where R_1 & R_2 are the d.c. path of Z_1 & Z_2.

These equations give the idealised voltage gain and output, deviations such as V_{IO}, CMMR and K_{SVR} can be calculated as separate inputs to modify the 'ideal' result.

Basic Non-inverting and a.c. Amplifier

Fig. 4.3 Non-inverting amplifier.



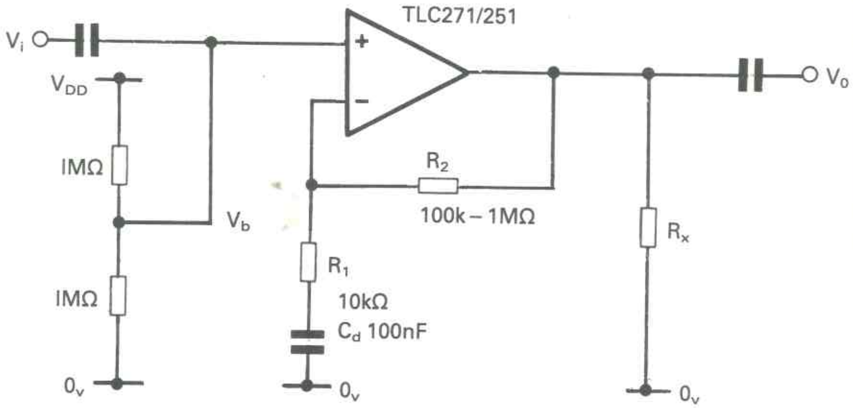
V_i is referenced to V_b.

$$V_o = \left(1 + \frac{R_2}{R_1}\right)\left(1 - \frac{1}{A\,\beta}\right) V1 + V_b$$

$$\beta = \frac{R_1}{R_1 + R_2}$$

gain error term =1 for very large A.

Fig. 4.4 Single rail A.C. amplifier.



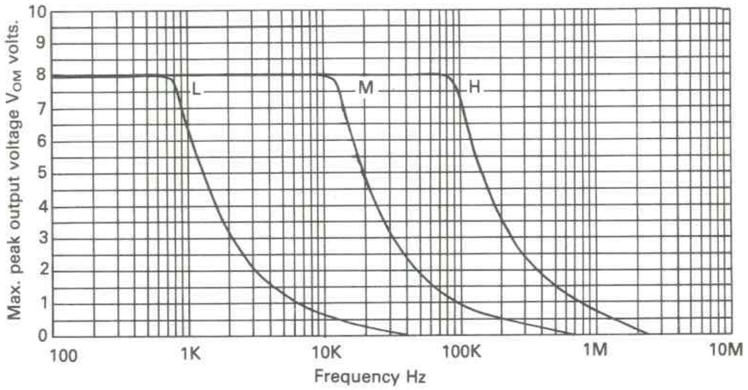
Decoupling capacitor Cd allows a high a.c. gain with unity d.c. gain keeping the output working point at $V_b \pm V_{IO}$. The inclusion of resistor Rx will improve the cross over distortion which may be encountered with the low and medium bias modes dependent on signal amplitude and frequency. The table gives some typical small signal (not slew limited) bandwidths for gains of 11 and 101 in the three bias modes with $V_{DD} = 5V$.

Table 4.1

Bias mode	**−3dB BW kHz @ gain 11**	**−3dB BW @ kHz gain 101**
Low	13.5	1.4
Medium	93.0	8.0
High	234.0	22.4

Large signal bandwidth is limited by slew rate considerations and Figure 4.5 shows typical plots for these at the three bias levels. This Figure shows that the large signal bandwidth imposes no limitations on the audio bandwidth at low values of closed loop gain for the high bias mode. The high bias mode also provides good quality audio output over this bandwidth in contrast to most bipolar single rail types.

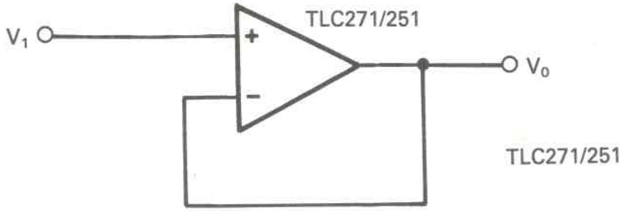
Fig. 4.5 Typical peak output voltage V_{OM} Vs. frequency.



An a.c. voltage follower is easily produced by replacing R_2 by a short circuit and removing R_1 and C_d. The low bias currents mean that high value bias resistors may be used eliminating the need for ‘bootstrapping’ to increase the bias circuit impedance.

Unity Gain Voltage follower.

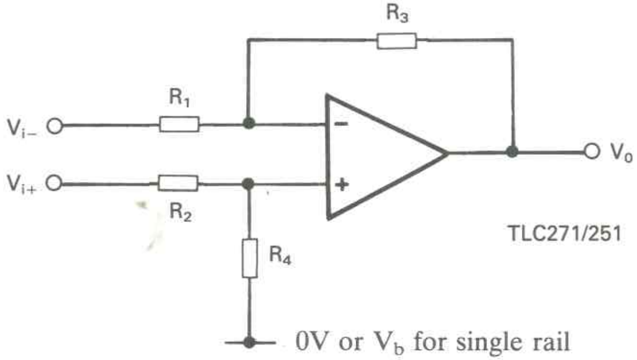
Fig. 4.6 Unity gain voltage follower.



$\frac{V_o}{V_i} = \left(1 - \frac{1}{A}\right)$ and gives 2μV/V output error in low bias mode and takes advantage of long term drift and temperature coefficient performance (0.1μV/month and 0.7μV/oC).

Differential Amplifier

Fig. 4.7 Differential amplifier.



This is the classical differential amplifier (subtractor) analysed as follows:

By superposition $V_o = \frac{R_4}{R_2 + R_4} \times \left(1 + \frac{R_3}{R_1}\right) \times V_{i+} - \frac{R_3}{R_1} \times V_{i-}$(1)

if $R_1 = R_2$ and $R_3 = R_4$

this reduces to $V_o = (V_{i+} - V_{i-}).\frac{R_3}{R_2}$

The disadvantages of this circuit are that it's input impedance is unbalanced and the common mode rejection is modified by the source impedances.

Common mode rejection is also compromised by resistor tolerances as illustrated:

$$\text{CMRR} = \left| \frac{\text{Differential Gain}}{\text{Common mode Gain}} \right| \text{ by definition.}$$

Substituting the common mode signal V in (1) gives common mode gain:

$$\frac{V_o}{V} = \left[\frac{R_4}{R_2 + R_4}\left(1 + \frac{R_3}{R_1}\right) - \frac{R_3}{R_2} \right]$$

substituting $R_3 = R_4 = 100\ R_1$ with $R_2 = 1.1\ R_1$ i.e. 10% mismatch gives $V_o/V = -0.099$

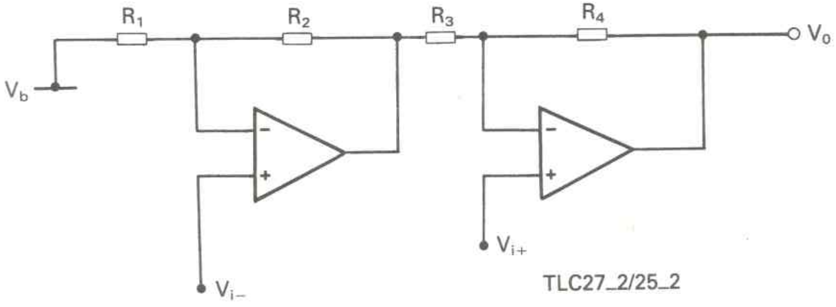
therefore $\text{CMRR} = \frac{100}{0.099} = 1010$ approx 60dB i.e. a nominal 20dB reduction in the op-amps normal specification.

Again higher values of resistance (i.e. 100kohms) can be used to implement the circuit, but a small value of capacitor across R_3 will be needed to prevent instability and overshoot in the transient response, particularly for the low and medium bias devices where phase margin degradation due to input poles has a greater effect. This circuit will operate with single rail by use of a suitably chosen bias V_b.

Two Op-amp Instrumentation Amplifier

A differential amplifier that has high and balanced input impedance and employs two op-amps (e.g. duals TLC272_/252_) is shown below:

Fig. 4.8 Two op-amp instrumentation amplifier.



By superposition:

$$V_o = \left(1 + \frac{R_4}{R_3}\right) V_{i+} - \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3} V_i \quad \text{(for } V_b{=}0\text{)}$$

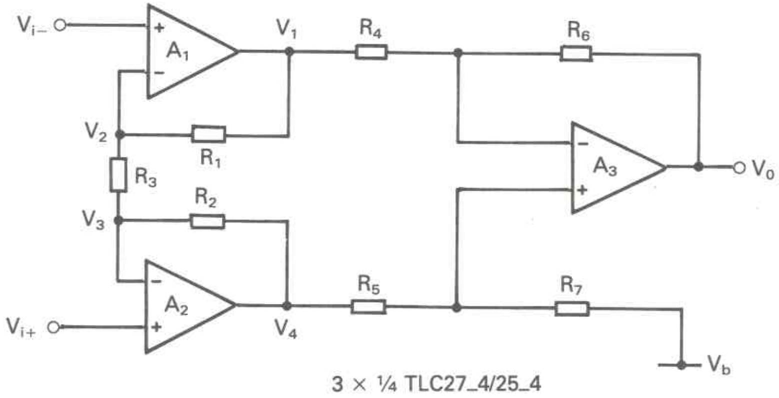
For $R_1 = R_4$ and $R_2 = R_3$ $\quad V_o = (V_{i+} - V_{i-}) \left(1 + \frac{R_1}{R_2}\right)$

The circuit has the same common mode rejection performance as the previous circuit. The main limitation to performance is in CMR to a.c. signals. This is caused by the V_{i-} input being bandlimited by two op-amps as opposed to one for the V_{i+} input.

Three Op-amp Instrumentation Amplifier

This is a differential amplifier that has high input impedance and overcomes the problem of mismatched CMR to a.c. signals.

Fig. 4.9 Three op-amp instrumentation amplifier.



With $V_b = 0V$ this is analysed as follows:

Assume $V_i- = 0$, then $V_2 = 0$ and $V_3 = V_{i+}$

therefore $V4 = V_{i+} \times \left(1 + \frac{R_2}{R_3}\right)$ and $V_1 = -V_{i+} \times \frac{R_1}{R_3}$

similarly if $V_{i+} = 0$

$V_1 = V_{i-} \times \left(1 + \frac{R_1}{R_3}\right)$ and $V_4 = -V_{i-} \times \frac{R_2}{R_3}$

by superposition $(V_4 - V_1) = (V_{i+} - V_{i-}) \left(1 + \frac{R_1 + R_2}{R_3}\right)$

if $R_6 = R_7$ and $R_4 = R_5$ then A3 functions as the basic differential amplifier and:

$$V_o = (V_{i+} - V_{i-}) \frac{R6}{R_4} \left(1 + \frac{R_1 + R_2}{R_3}\right)$$

Matching around A3 determines CMRR as described previously and differential gain can be controlled by R_3. Optimisation of CMR can be achieved by adjustment of R_7.

This amplifier can be built from a quad op-amp, TLC27_4/TLC25_4 where _ denotes bias mode. For example, if the application common mode range allowed, a really low power (8μW at 1V V_{DD}), slow speed (enough for a temperature sensor with slew rate of 0.001V/μs), high impedance interface circuit could be built using a TLC25L4. This example is at the extreme in terms of power, speed and voltage ranges but demonstrates the possibilities.

The spare op-amp in the quad package may be used to enhance circuit performance. Connected as an inverting amplifier driven from V_o it can provide more gain. Connected as a voltage source (Figure 4.10) it can be used to drive V_b without affecting common mode rejection and connected as Figure 4.11 it can be used as a shield-guard drive to reduce the capacitive effects of input cables.

Fig. 4.10 Low impedance bias voltage circuit.

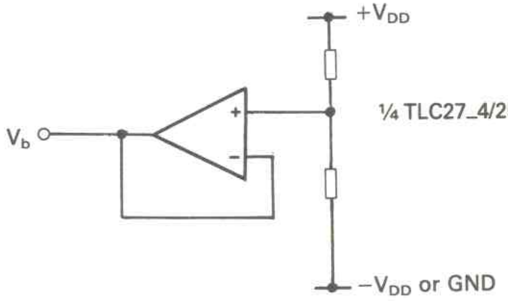
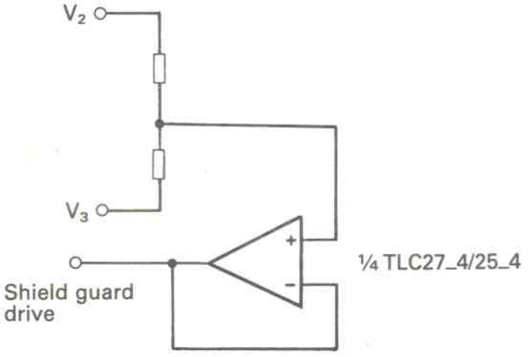


Fig. 4.11 Shield guard drive circuit.

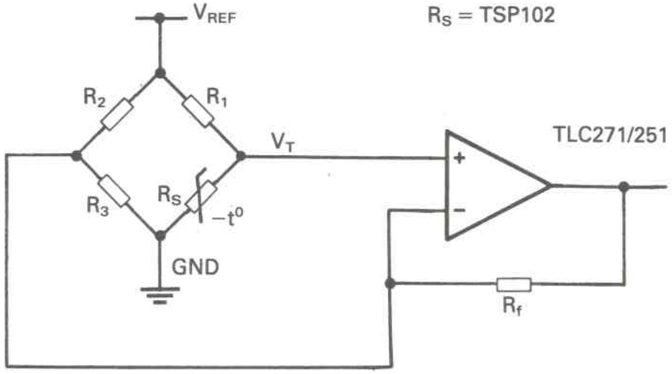


Again with higher value feedback resistors, particularly in the low and medium bias modes, small value capacitors across the feedback resistors may be necessary to ensure stability.

Bridge Amplifier

Basic circuit

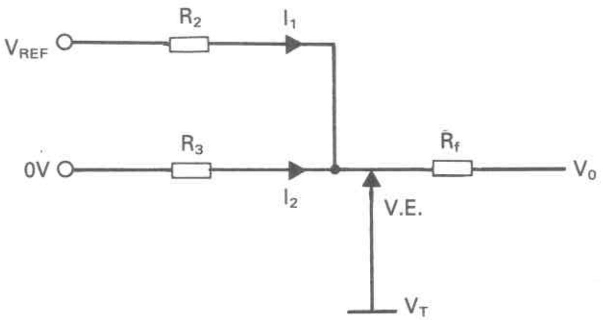
Fig. 4.12 Bridge amplifier used to sense temperature.



The differential output voltage of the bridge is forced to zero by the feedback connection. The amplifier is used to measure the current flow under these conditions.

The circuit can be analysed using 'virtual earth' analysis with the earth at potential V_T:

Fig. 4.13 Virtual earth bridge analysis.



$$V_T = \frac{V_{ref}R_s}{R_1 + R_2}$$

$$I_1 = \frac{V_{ref} - V_T}{R_2}; \quad I_2 = -\frac{V_T}{R_3}; \quad \frac{V_o - V_T}{R_f} = -(I_1 + I_2)$$

Therefore $V_o = V_T - R_f(I_1 + I_2)$

$$= V_T + R_f.\left(\frac{V_T}{R_3} - \frac{V_{ref} - V_T}{R_2}\right)$$

Re-arranging for V_T and putting $R_1 = R_2 = R_3 = R$

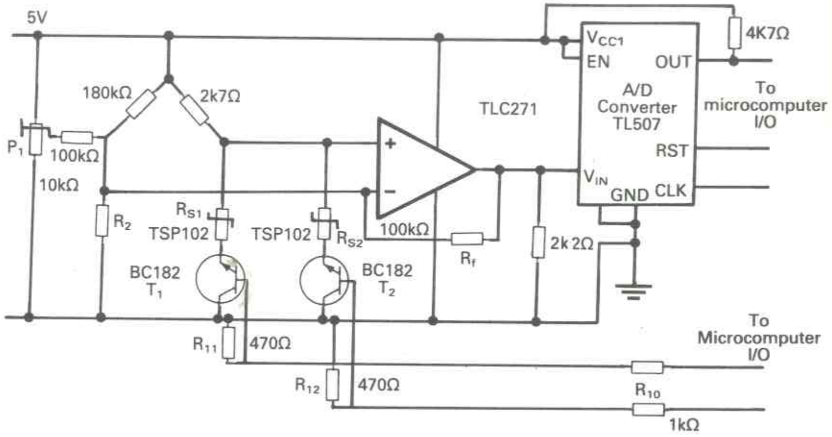
$$V_o = V_T\left(1 - \frac{2R_f}{R}\right) - \frac{V_{ref}R_f}{R}$$

substituting for V_T and $R_s = R(1 + d)$

$$V_o = V_{ref} \times \frac{R_f}{R} \times \frac{d}{1 + d} \quad \text{For } d << 1 \quad V_o = V_{ref} \times \frac{R_f}{R} \times \frac{d}{2}$$

As the input bias current of the LinCMOS op-amps are so small it is not necessary to include a resistor from (+) input to 0V. to balance input currents. Figure 4.14 shows this circuit used in a typical application.

Fig. 4.14 Temperature sensor interface.



Output Current Booster Amplifiers

Various configurations can be used to boost output current capability, three of which are shown here:

Figure 4.15 shows a single rail amplifier feeding current to a load connected to GND.

Fig. 4.15 Single rail current booster feeding to ground.

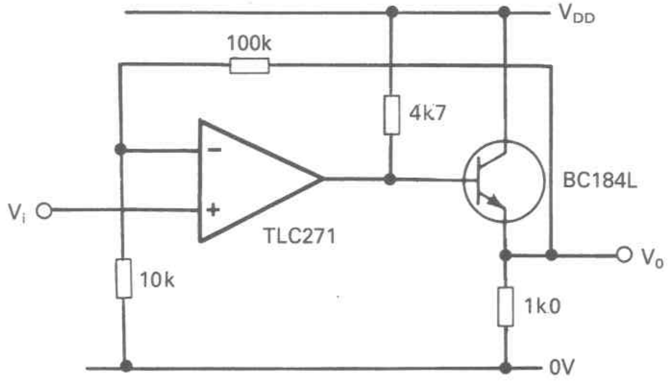
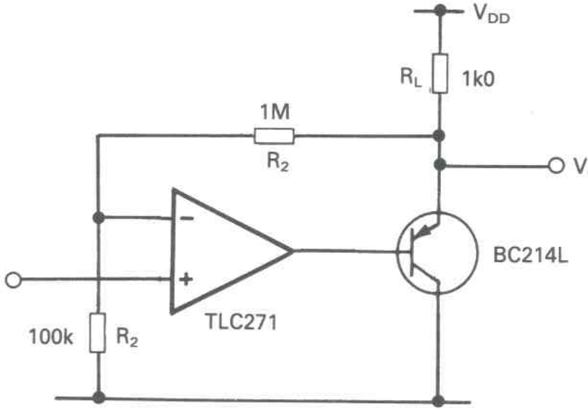


Figure 4.16 shows a single rail amplifier feeding current to a load connected to V_{DD}.

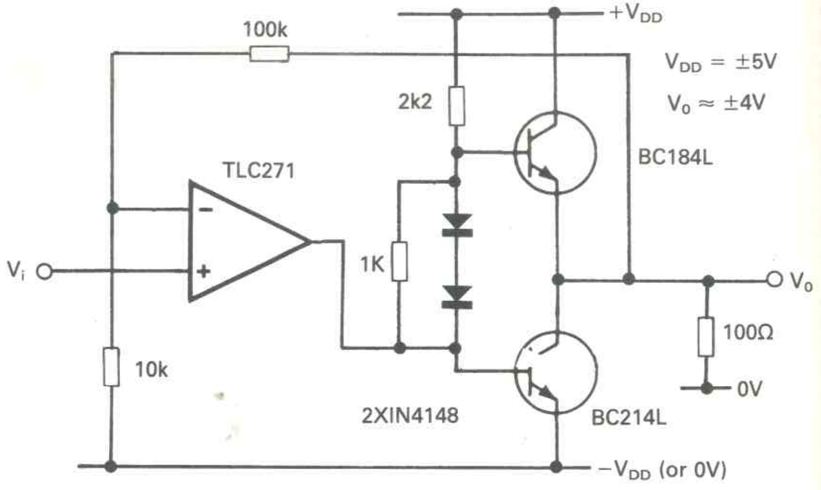
Fig. 4.16 Single rail current booster feeding to $+V_{DD}$.



$$V_{OM} = \frac{V_{DD} R_L}{R_L + R_1 + R_2}$$

Figure 4.17 shows a +/− supply rail amplifier.

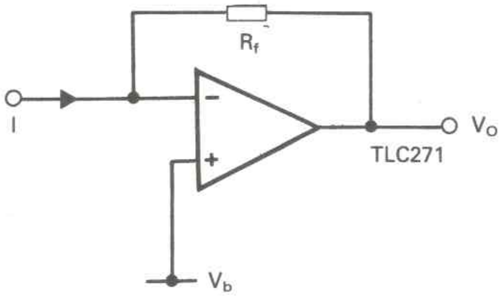
Fig. 4.17 ± supply booster amplifier.



Current Amplifiers

The basic current to voltage converter is shown in Figure 4.18 R_f causes a 'virtual earth' at (−) input thus $V_O = -IR_f$.

Fig. 4.18 Basic current to voltage converter.



Current Sink

Low op-amp bias current and low V_{IO} selections (AC = 5mV max. & BC = 3mV max.) allow precision low current sink circuits as shown in Figure 4.19. The common mode range to 0V on the inputs allows wide control range. Figure 4.20 shows a circuit for larger current sink capability.

Fig. 4.19 Precision low current sink.

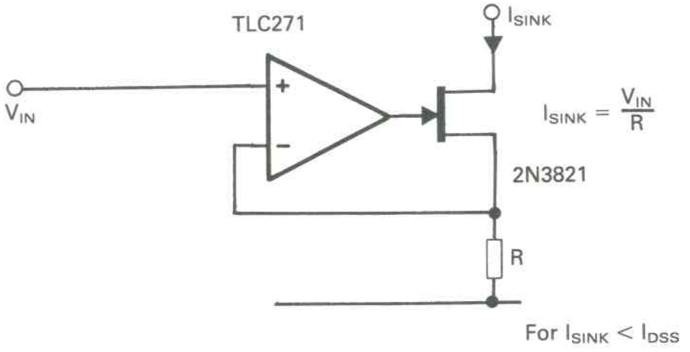
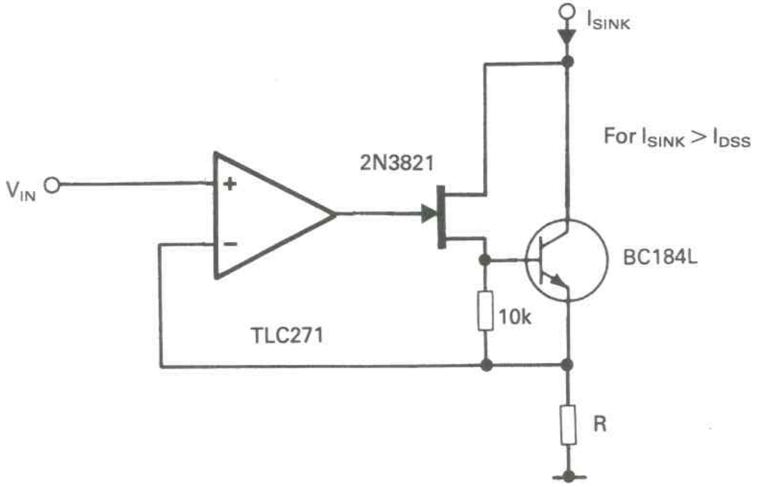


Fig. 4.20 Higher current sink.



Current Source

Figures 4.21 to 4.24 show four different configuration of current source.

Fig. 4.21 Positive current source.

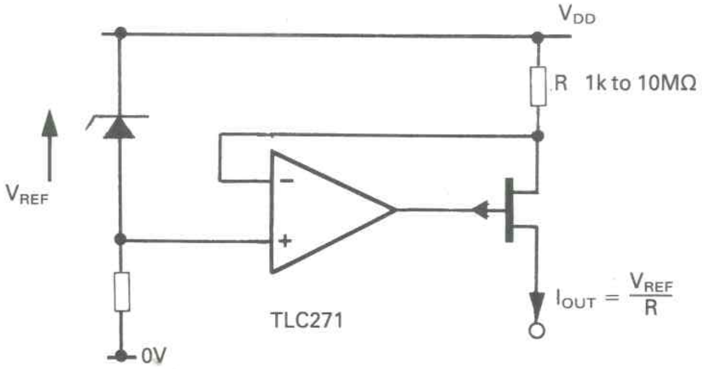


Fig. 4.22 Non-inverting floating load current source.

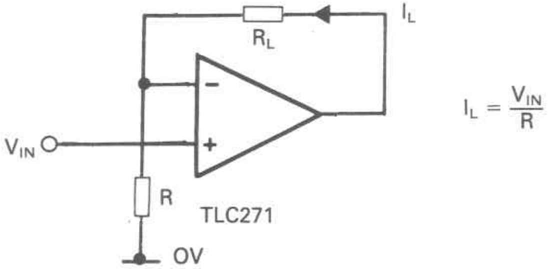
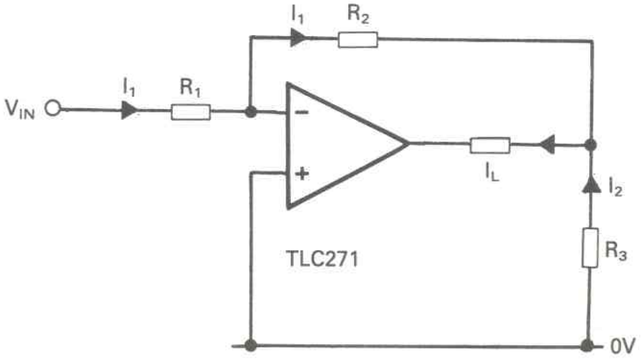


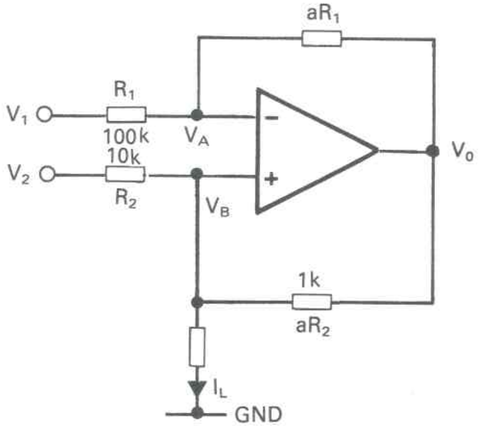
Fig. 4.23 Inverting floating load current source.



$$I_1R_2 = I_2R_3 \ \& \ I_1 = \frac{V_{in}}{R_1}$$

$$\therefore I_L = I_1 + I_2 = I_1\left(1 + \frac{R_2}{R_3}\right) = \frac{V_{in}}{R_1}\left(1 + \frac{R_2}{R_3}\right)$$

Fig. 4.24 Earthed load current source.



$$\frac{V_1 - V_A}{R_1} = \frac{V_A - V_o}{aR_1} \quad \therefore V_o = V_A(1 + a) - aV_1$$

$$\therefore I_L = \frac{V_2 - V_B}{R_2} + \frac{V_o - V_B}{aR_2}$$

$$= \frac{V_2 - V_B}{R_2} + \frac{V_A(1 + a) - aV_1 - V_B}{aR_2}$$

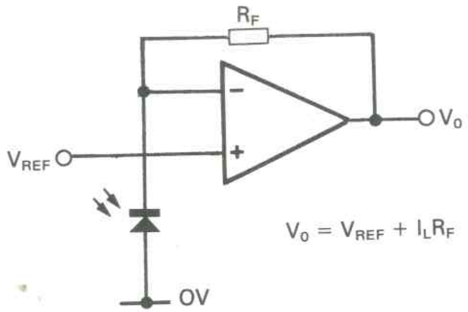
but $V_A = V_B \therefore I_L = \dfrac{V_2 - V_1}{R_2}$

For single input control put V_1 input to ground.

Basic Photo Diode Receiver

The basic circuit is shown in Figure 4.25. The non-inverting input is held at V_{ref}, and the feedback resistor R_F causes a virtual earth at the inverting input. This defines the reverse bias across the photo diode. The very low input bias currents of the LinCMOS op-amps do not mask the dark current of the photo diode as can occur with bipolar op-amps. Thus the circuit can be used for detecting low light intensities.

Fig. 4.25 Basic photo diode receiver.



COMPOSITE LOW DRIFT AMPLIFIERS

Fast Low Drift Amplifier Using TLC271 and LM318

Op-amps in composite connections are cost effective solutions where amplifiers with both high slew rate and good offset voltage specifications are required. Figure 4.26 shows the TLC271 with its low off-set drift teamed with the LM318's 50V/μs slew rate. The TLC271 is used, where it has best drift performance, in low bias mode. Typical instrumentation applications are in fast rectifiers and logarithmic converters.

At d.c., using the large loop gain of the TLC271, the output voltage drift is equal to the TLC271 input offset drift multiplied by the non-inverting gain of the LM318. The offset voltage of the LM318 is continuously nulled by forcing the summing node to equal the offset of the TLC271. This is achieved by the use of a secondary feedback loop formed by R_1, R_2 and the LM318's input stage.

Fig. 4.26 Fast low drift amplifier.

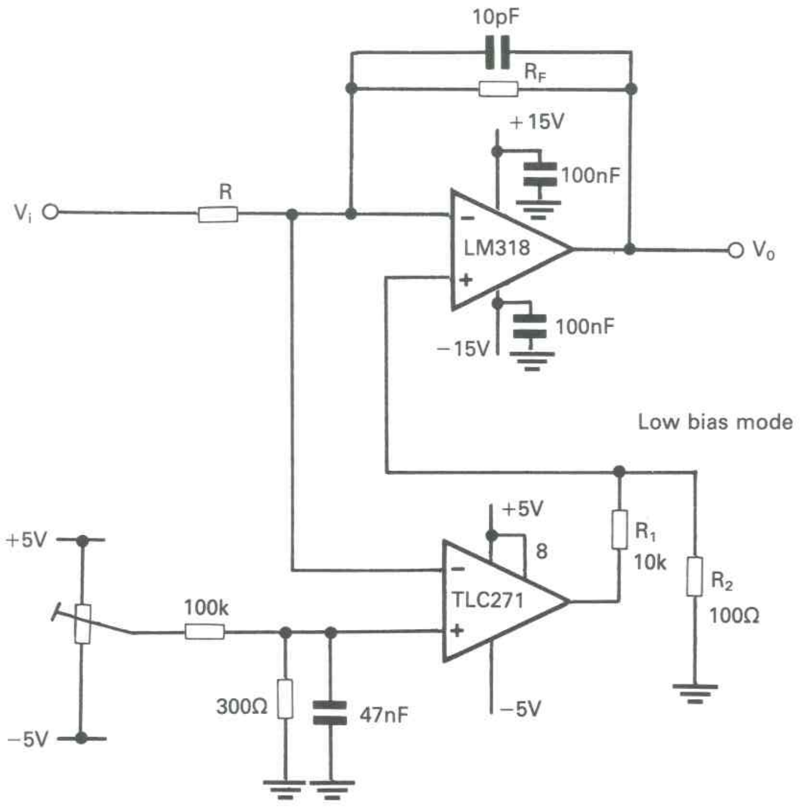
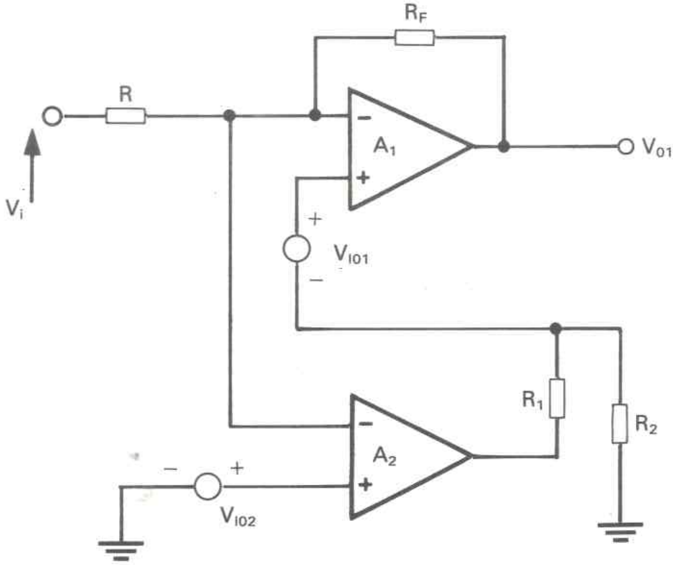


Figure 4.27 shows the d.c. feedback loop analysed for offset voltage drift as follows assuming $V_i = 0$:

$$V_{01} = \left[-V_{01} \frac{R}{R + R_F} + \left(-V_{01} \frac{R}{R + R_F} + V_{I02} \right) A_2 \frac{R_2}{R_1 + R_2} + V_{I01} \right] \times A_1$$

Rearranging with assumptions that: $\frac{1}{A_1} << 1$ & $A_2 \frac{R_2}{R_1 + R_2} >> 1$

Fig. 4.27 Fast low drift amplifier D.C. analysis.



$$V_{01} = \left(1 + \frac{R_F}{R}\right)\left[V_{I02} + \frac{V_{I01}}{A_2}\left(1 + \frac{R_1}{R_2}\right)\right]$$

If $\frac{V_{I01}}{A_2}\left(1 + \frac{R_F}{R}\right) << V_{I02}$ and

$$\frac{dV_{I01}/dT}{A_2}\left(1 + \frac{R_1}{R_2}\right) << dV_{I02}/dt$$

Then: $V_{01} = \left(1 + \frac{R_F}{R}\right)V_{I02}$; $\frac{dV_{01}}{dT} = \left(1 + \frac{R_F}{R}\right)\frac{dV_{I02}}{dT}$

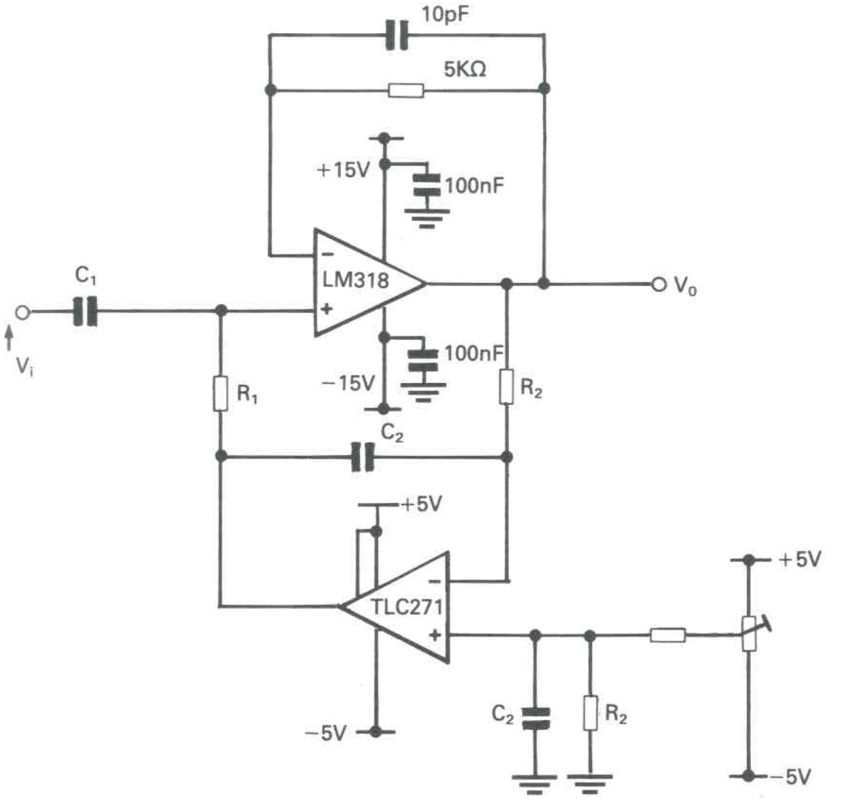
The error due to bias current drift is dominated by the LM318 where $V_{01} = R_F.I_{IB}$ (LM318) $\therefore$ $dV_{01}/dT = R_F \,.\, dI_{IB}/dT$ and limits the practical values of feedback resistors to a few kohms.

Fast Low Drift AC. Buffer using TLC271 and LM318

A composite connection has advantages in applications where a fast a.c. buffer is required and d.c. output error voltage cannot be tolerated.

Examples of such circuits are sample and hold and A/D converters. A composite circuit using a TLC271 and LM318 is shown in Figure 4.28.

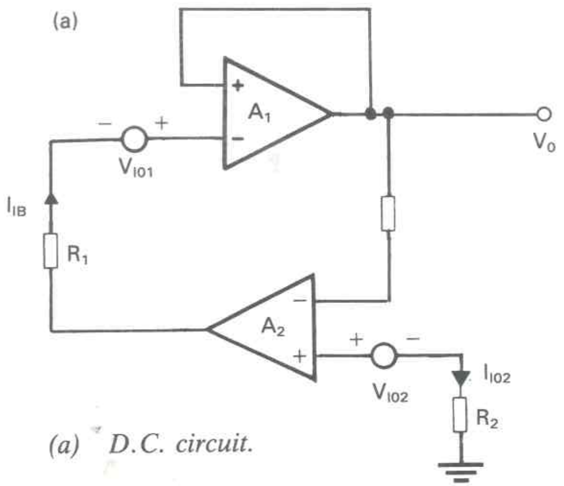
Fig. 4.28 Fast low drift A.C. buffer.



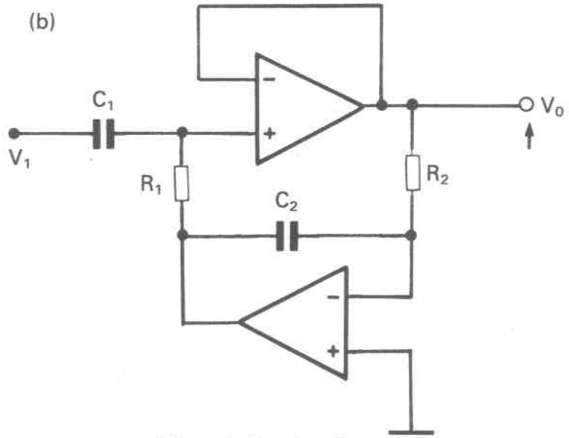
The output voltage V_0 is integrated by R_2C_2 and compared to zero volts by TLC271. The difference, integrated again by R_1C_1, adjusts the input d.c. level of the LM318 noninverter connected amplifier to give zero d.c. output voltage. A reasonable choice of R_2 will give an output offset drift equal to the TLC271 specification. The zeroing circuit forms an active second order highpass filter from V_i to V_o.

Figure 4.29 (a) & (b) show the d.c. and a.c. circuits respectively.

Fig. 4.29



(a) D.C. circuit.



(b) A.C. circuit

The d.c. conditions of Figure 4.29(a) are analysed assuming R_{in} of $A_2 >> R_2$ equating voltages at node A:

$$V_O - V_{IO1} + I_{IB}R_1 = (-V_O + V_{IO2} + I_{IO2}R_2)A_2$$

If A_2 tends to infinity then:

$$V_O = V_{IO2} + I_{IO2}R_2 \quad \& \quad \frac{dV_O}{dT} = \frac{dV_{IO2}}{dT} + R_2\frac{dI_{IO2}}{dT}$$

The a.c. analysis of Figure 4.29(b) yields:

$$\frac{V_O}{Vi} = \frac{s^2}{s^2 + (1/R_1C_1)s + (1/R_1R_2C_1C_2)} = \frac{s^2}{s^2 + s(\omega_O/Q) + \omega_O{}^2}$$

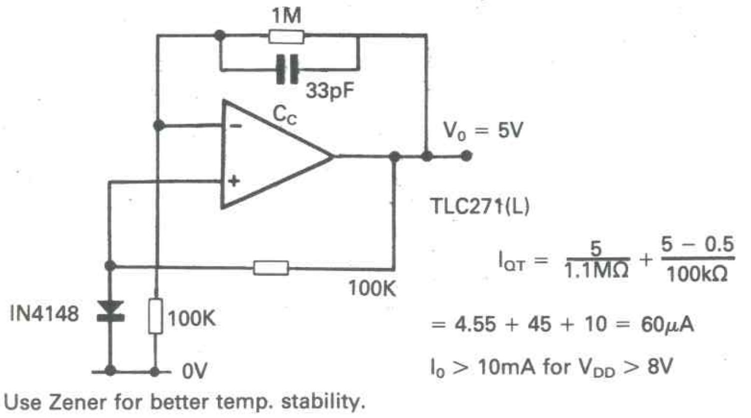
$$\text{then: } Q = \left(\frac{R_1C_1}{R_2C_2}\right)^{1/2} \quad \& \quad \omega_o = (R_1R_2C_1C_2)^{-1/2}$$

Choose C_1 and C_2; then $R_1 = Q/C_1\omega_o$ & $R_2 = 1/C_2Q.\omega_o$

VOLTAGE REGULATORS

Figure 4.30 shows a low quiescent power voltage regulator that consumes only 60µA of standby current using the low bias mode. A load regulation of 10% can achieved for the values shown. Capacitor C_c is included to prevent instability which manifests itself by higher than expected quiescent current.

Fig. 4.30 Low power voltage regulator.



$$I_{QT} = \frac{5}{1.1M\Omega} + \frac{5 - 0.5}{100k\Omega}$$

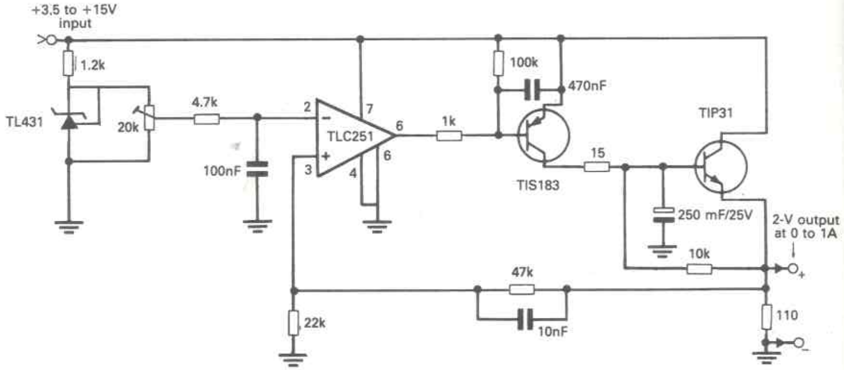
$$= 4.55 + 45 + 10 = 60\mu A$$

$I_o > 10mA$ for $V_{DD} > 8V$

Use Zener for better temp. stability.

Figure 4.31 shows a low voltage regulator circuit employing a TLC251 1V op-amp. There is seldom need to design a new regulator with the variety of monolithic regulators now available. However many new devices, such as gate arrays and logic circuits, require a regulated voltage as low as 2–3 volts. Gate arrays require a well regulated supply of 2 volts at typical current of 250mA. With several of these devices in a system a current of 1A may be needed from a wide input voltage range, particularly 5V or less. In such applications the TLC251 can provide the loop gain needed to give a regulation of ±20mV over the 1A load range.

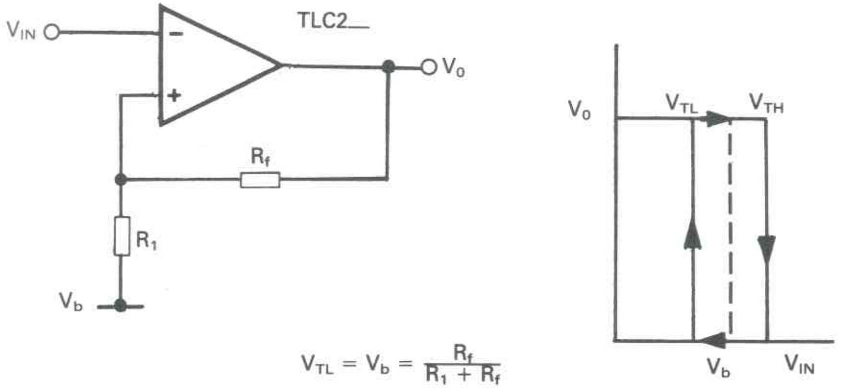
Fig. 4.31 2V voltage regulator.



BASIC SCHMITT TRIGGER

An example is shown in Figure 4.32 for single rail operation centred on V_b. For symmetrical operation V_b should be $V_{OM}/2$.

Fig. 4.32 Basic Schmitt trigger.



$$V_{TL} = V_b = \frac{R_f}{R_1 + R_f}$$

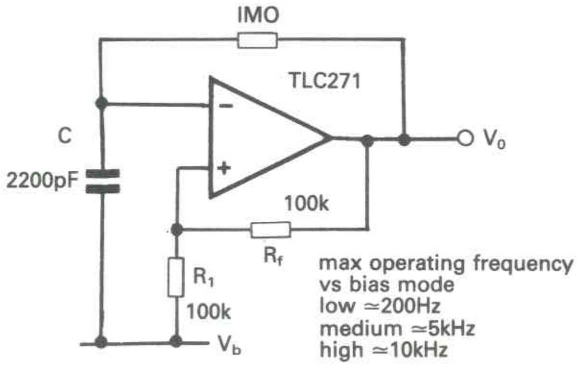
$$V_{TH} = V_b \frac{R_f}{R_1 + R_f} + \frac{V_{OM}\, R_1}{R_1 + R_f}$$

OSCILLATOR CIRCUITS

Astable Squarewave

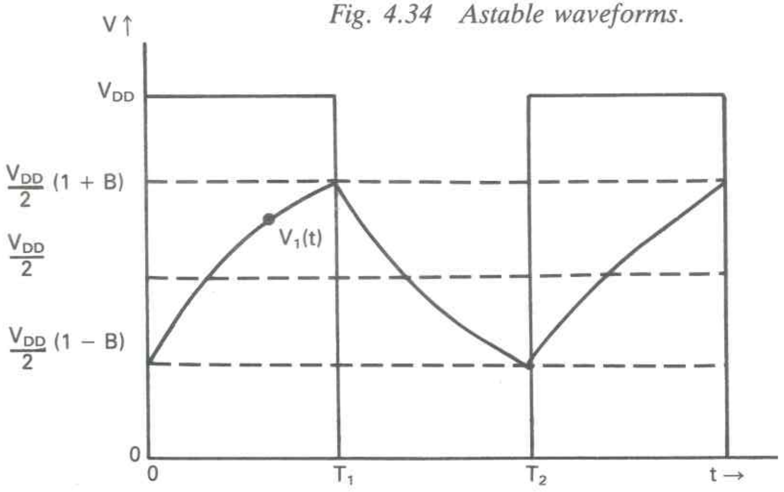
Adding a RC network to a Schmitt trigger forms the classic op-amp astable op-amp astable circuit. (Figure 4.33).

Fig. 4.33 Astable oscillator.



max operating frequency
vs bias mode
low ≃200Hz
medium ≃5kHz
high ≃10kHz

Fig. 4.34 Astable waveforms.



The waveforms for single rail operation, assuming V_o can swing between V_{DD} and 0V, are shown in Figure 4.34. The circuit is analysed as follows:

V_1 as a function of time $V_1(t)$ is given by:

$$V_1(t) = \left(V_{DD} - \frac{V_{DD}}{2}(1 - B)\right)(1 - e^{-t/CR}) + \frac{V_{DD}}{2}(1 - B) \quad (1)$$

at T_1; $V_1 = \frac{V_{DD}}{2}(1 + B)$ equating to (1) and simplifying.

$$(1 + B) - (1 + B)e^{-T_1/C.R} = 2B$$

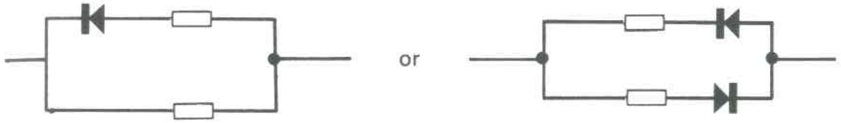
therefore $T_1 = CR\ln\left(\frac{1 + B}{1 - B}\right)$ but $B = \frac{R_1}{R_f + R_1}$

therefore $T_1 + T_2 = T_p = 2CR\ln\left(\frac{2R_1 + R_f}{R_f}\right)$

and for $R_1 = R_f$ $\quad T_p$ approx. $= 2.2CR$

Thus the frequency is independent of the supply voltage V_{DD}. As in practice V_o swings from 0V to V_{OM} then to achieve a symmetrical waveform the bias should be adjusted to $V_{OM}/2$ or back to back zeners should be placed across R_f to limit the output swing. There are variations to this circuit for asymmetrical operation by replacing the feedback resistor with diode/resistor combinations to control the capacitor changing rate as shown in Figure 4.35.

Fig. 4.35 Astable feedback alternatives.



The low input bias currents of the LinCMOS op-amps allow high values of resistor and lower non-electrolytic values of capacitor for high accuracy and wide mark-space ratios. Minimum pulse widths achievable will be determined by op-amp slew rate performance and hence for the smallest pulses high bias mode should be used.

Single Rail VCO

A voltage controlled oscillator that operates on a single rail is shown in Figure 4.36.

Op-amp A_1 operates as an integrator with an input voltage $\pm V_{in}/2$ set by voltage divider R_1 and R_2, integrating from $+V_{in}/2$ when TR1 is off and $-V_{in}/2$ when TR1 is on. By making $R_4 = \frac{1}{2}R_3$ integrating currents are equal for each period. Figure 4.37 shows the waveforms and the frequency of oscillation is derived as follows:

During time T_1; $\quad V_1(t) = -\frac{V_{in}}{2CR}t + \frac{V_{DD}}{2}(1 + B)$

at T_1; $\quad V_1 = \frac{V_{DD}}{2}(1 - B)$

Fig. 4.36 Voltage controlled oscillator.

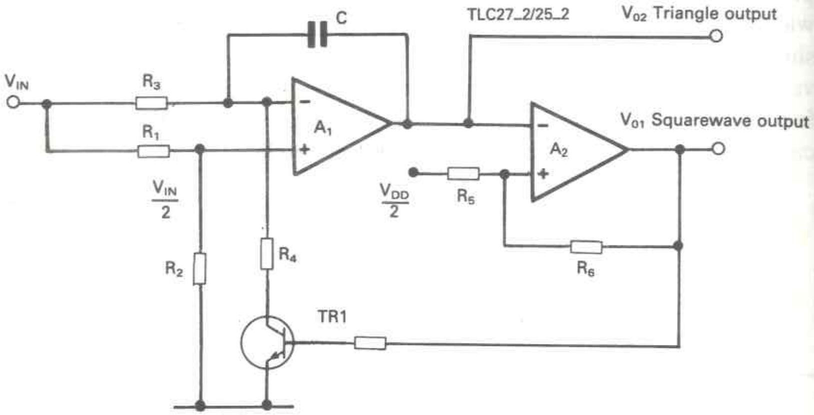
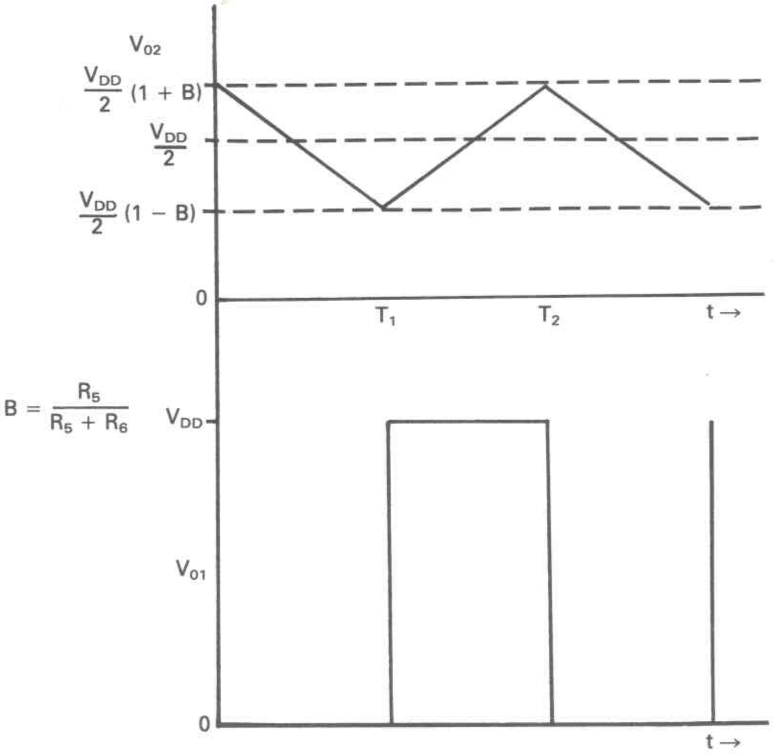


Fig. 4.37 Waveforms.

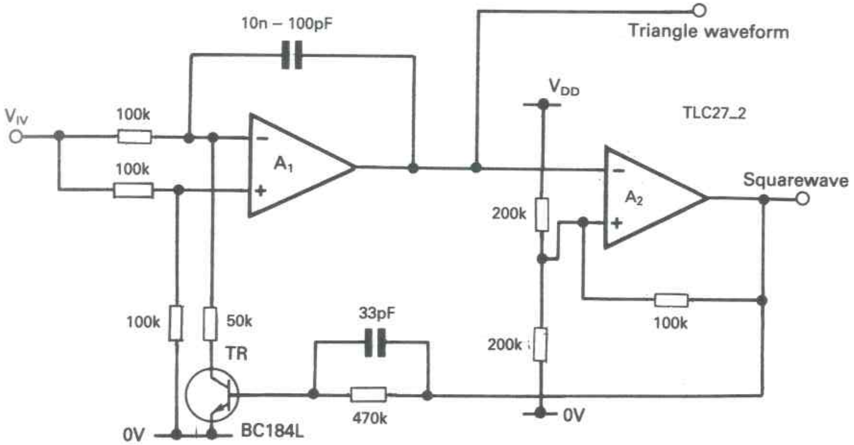


$$\text{therefore } \frac{V_{DD}}{2}(1 - B) = -\frac{V_{in}T_1}{2CR} + \frac{V_{DD}}{2}(1 + B)$$

$$\text{therefore } T_1 = \frac{2CRV_{DD}.B}{V_{in}} \quad \text{or} \quad f_{osc} = \frac{V_{in}(R_5 + R_6)}{4CRV_{DD}R_5}$$

Thus the frequency of operation is proportional to input voltage V_{in}. See Figure 4.38 for a circuit with some typical component values.

Fig. 4.38 VCO with typical values.



base low bias 200Hz
medium bias 5KHz
high bias 30KHz
} Slew rate limited

Asymmetry is due to TR switching times.

Wien Bridge Sinewave Oscillator

The classic low distortion sine wave oscillator is shown in Figure 4.39.

Fig. 4.39 Wien bridge oscillator.

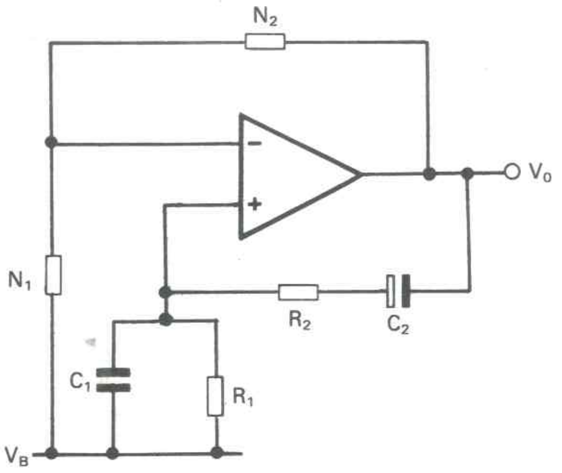
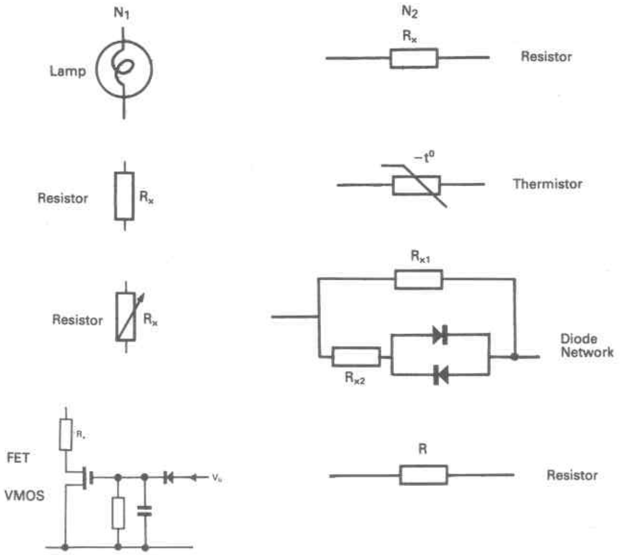


Fig. 4.40 Typical feedback combinations for Wien oscillator.



This has a frequency of oscillation $f_o = 1/[2\pi\sqrt{R_1R_2C_1C_2}] = 1/(2\pi RC)$ for equal component values. The attenuation of this feedback circuit at zero phase shift is 1/3 and thus the amplifier must provide a gain of exactly 3 to sustain oscillations. This is achieved by automatic amplitude control which provides an amount of negative feedback dependent on the output amplitude. Thus the circuit will oscillate at any output amplitude that satisfies the gain of 3 requirement.

Figure 4.40 shows a selection of feedback networks that have been used for gain control i.e. incandescent lamp (+ve temp coef), thermistor −ve temp coef), diode networks and n-channel junction and VMOS FETs.

Fig. 4.41 Wien oscillator with typical values.

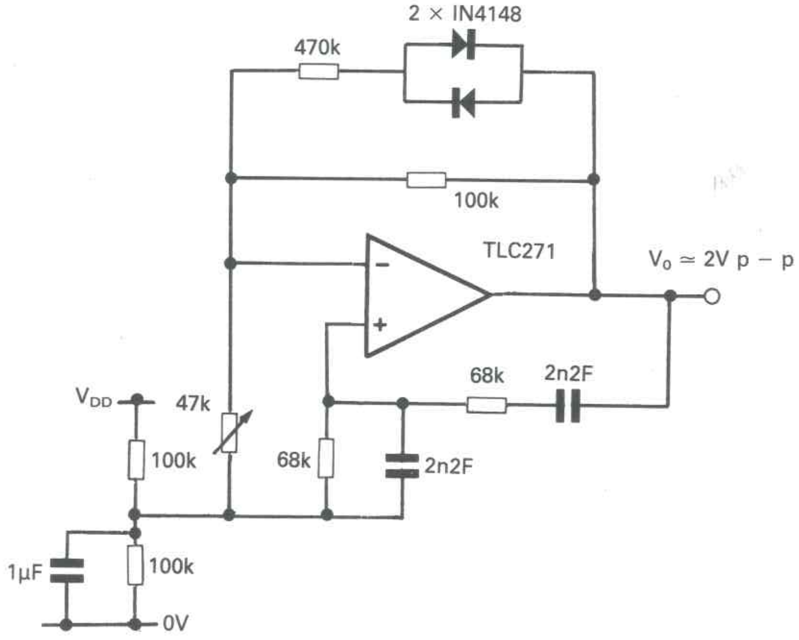


Figure 4.41 shows a circuit with typical values for a diode feedback network, the usual A_{OL}/A_{CL} gain ratio and slew rate considerations should be made at the operating frequency.

ACTIVE FILTERS

Introduction

Active filters employ op-amps with passive resistive and capacitive components to synthesise filters with the characteristics of lumped R-L-C circuits. Essentially this allows the resonance effects of R-L-C circuits to be reproduced by passive and active components using energy from the power supply. This can be understood in terms the pole-zero diagram where the poles of passive R-C networks, that lie on the negative real axis, are moved into the complex plane to form conjugate pairs. Thus the desirable characteristics of R-L-C networks are achieved.

Active filters have many advantages over their R-L-C counterparts especially at low frequencies where the elimination of large inductors improves filter performance while reducing cost. Other advantages are greater response accuracy and the ability to provide circuit gain.

LinCMOS op-amps provide user benefits for the implementation of active filters. At low frequencies their very low bias currents allow the use of higher value resistors and hence lower value capacitors, of closer tolerance. While the greater bandwidth and slew rate of high bias mode allows filters to be designed that operate at higher frequencies than those constructed using standard bipolar op-amps.

Designing active filters revolves around solving two major problems: these are usually called the approximation and realisation problems respectively. The approximation problem involves choosing a filter shape that satisfies the requirement in terms of amplitude, phase and transient response. The realisation problem is about finding and using a circuit topology that produces the chosen response, constrained by practical component characteristics and tolerances.

The following is an outline to the solution of these problems. For a greater understanding the reader should consult the references.*

---

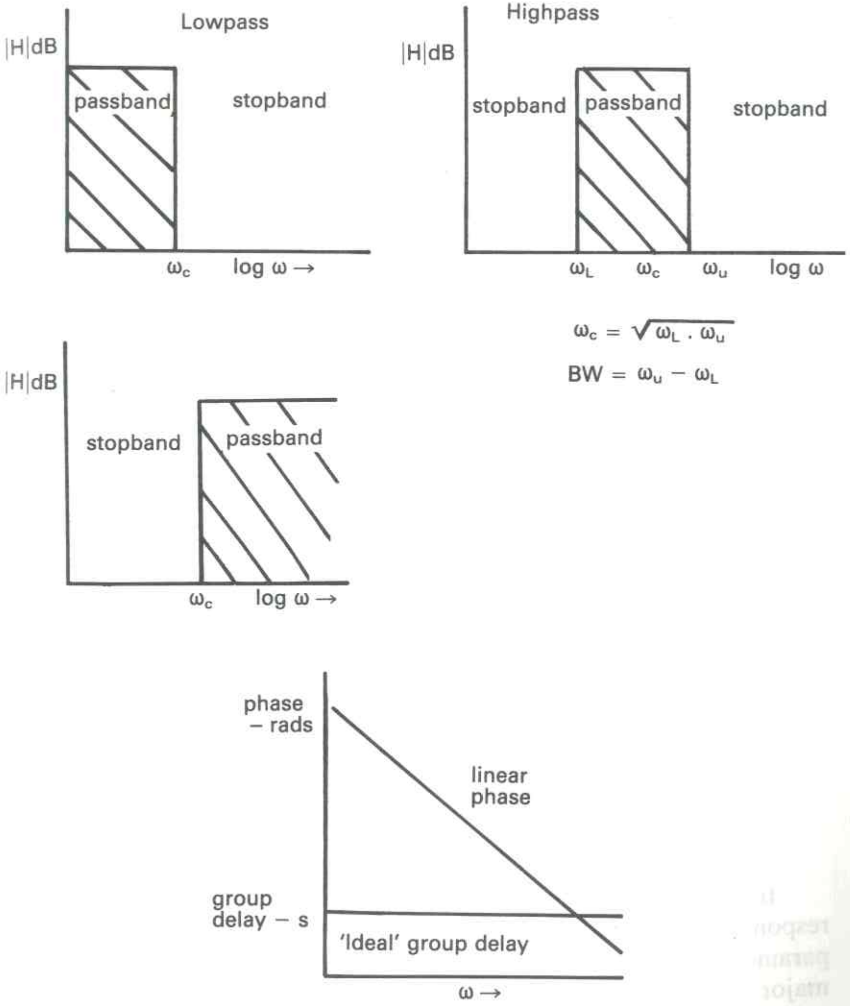
*see references 2 to 7

Approximation Problem

Ideal Response

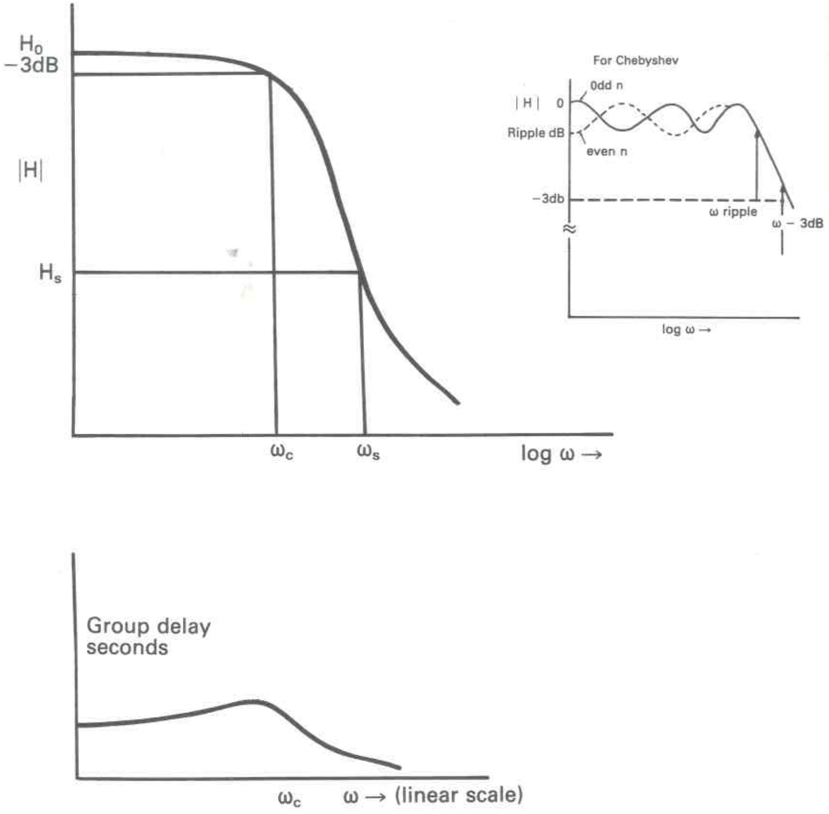
The ideal "brickwall" filter is represented by constant amplitude and group delay (linear phase) in the passband and zero transmission in the stopband (Figure 4.42).

Fig. 4.42 Ideal 'Brickwall' filter responses.



Practical filters have amplitude deviations in the passband, varying amounts of slope in the transition from passband to stopband and finite stopband transmission. Group delay (phase response), unless specifically optimised, will be non-linear particularly at the band edges. (Figure 4.43).

Fig. 4.43 Practical filter responses.



In general it is only possible to optimise one parameter of a filter's response be it amplitude, phase or transient response while the other parameters are compromised. The following is a description of the major "classical" filter transfer function shapes.

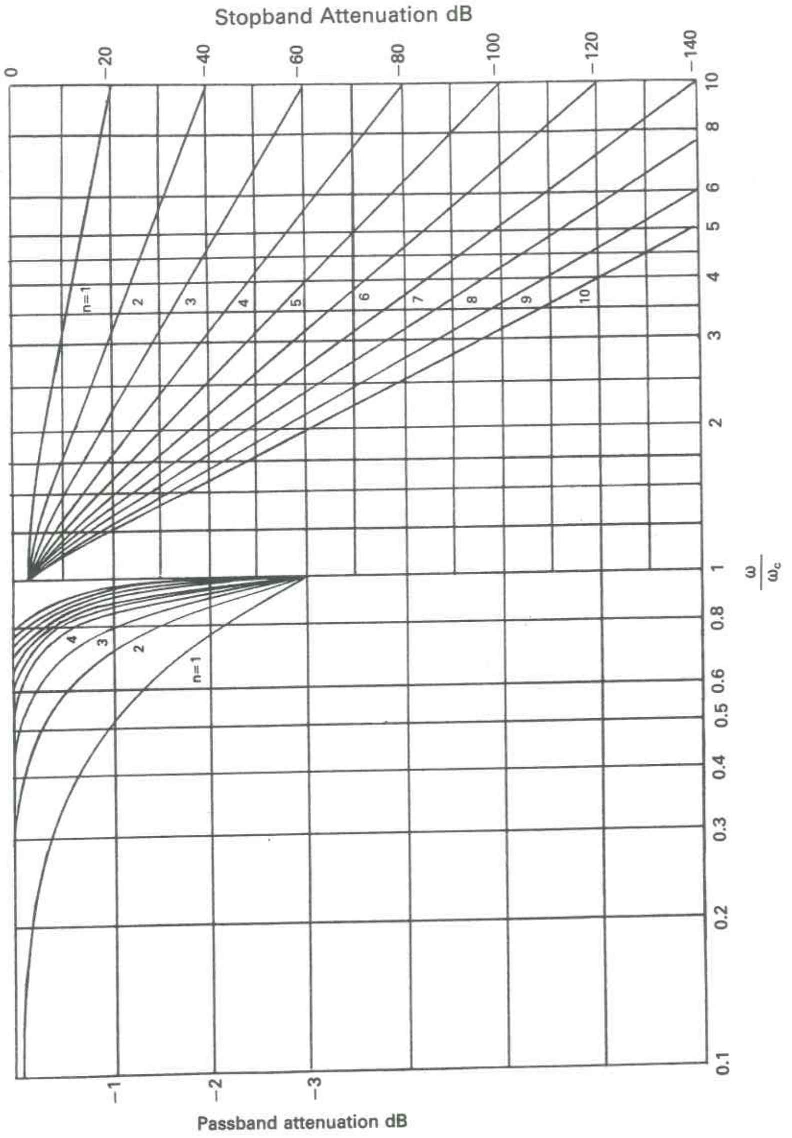


Fig. 4.44 Butterworth attenuation characteristic.

Butterworth-Maximally Flat Amplitude

The Butterworth shape is "maximally flat" and proceeds smoothly from the passband, without ripple, through the cut-off frequency f_c at −3dB into the stop band. For a lowpass filter this means zero error at low frequency. For a bandpass or highpass filter a ripple free "maximally flat" response is obtained. The Butterworth filter response displays a good compromise between all parameters and is a good first choice general purpose filter. Figure 4.44 shows the attenuation characteristics and Figures 4.45 (a) & (b) show delay and transient response respectively.

Fig. 4.45(a) Group-delay characteristics for Butterworth filters.

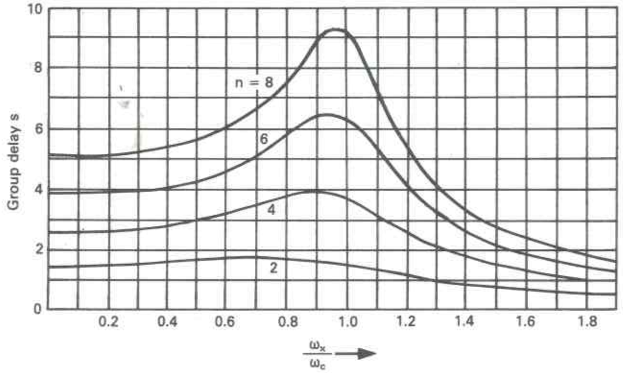
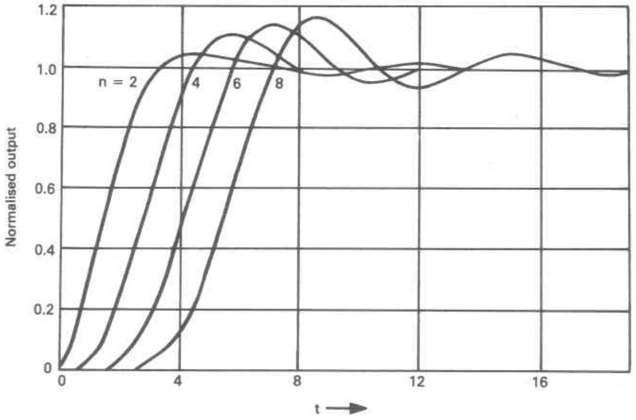


Fig. 4.45(b) Normalised step response for Butterworth filters.



The amplitude response H of a Butterworth filter is given by:

$$|H(j\omega)| = \frac{H_o}{[1 + (\omega/\omega_c)^{2n}]^{1/2}}$$

Normalised attenuation $A = [1 + (\omega/\omega_c)^{2n}]^{1/2}$.

Rearranging this, the order of filter n can be determined for slope factor ω_s/ω_c at attenuation $H_s = A$

$$n \geqslant \frac{\log (A^2 - 1)}{2\log (\omega_s/\omega_c)}$$

$$\text{For A in dB's } n \geqslant \frac{\log (10^{Adb/10} - 1)}{2\log (\omega_s/\omega_c)}$$

where ω_c is −3dB filter bandwidth in rads-sec.

The attenuation rate beyond cut-off ω_c is n × −20dB/decade. The pole positions for the Butterworth filter are given in Table 4.2(a).

Table 4.2 Butterworth & Bessel pole locations.

	(a) Butterworth Pole Locations		**(b) Bessel Pole Locations**	
Order n	Real Part $-\alpha$	Imaginary Part $\pm j\beta$	Real Part $-\alpha$	Imaginary Part $\pm j\beta$
2	0.7071	0.7071	1.1030	0.6368
3	0.5000 1.0000	0.8660	1.0509 1.3270	1.0025
4	0.9239 0.3827	0.3827 0.9239	1.3596 0.9877	0.4071 1.2476
5	0.8090 0.3090 1.0000	0.5878 0.9511	1.3851 0.9606 1.5069	0.7201 1.4756
6	0.9659 0.7071 0.2588	0.2588 0.7071 0.9659	1.5735 1.3836 0.9318	0.3213 0.9727 1.6640
7	0.9010 0.6235 0.2225 1.0000	0.4339 0.7818 0.9749	1.6130 1.3797 0.9104 1.6853	0.5896 1.1923 1.8375
8	0.9808 0.8315 0.5556 0.1951	0.1951 0.5556 0.8315 0.9808	1.7627 0.8955 1.3780 1.6419	0.2737 2.0044 1.3926 0.8253

normalised to 1 ohm & 1 rad/sec at −3dB

Chebyshev Equiripple Passband

Chebyshev transfer function shapes show greater selectivity close to the cut-off frequency than either Butterworth or Bessel (see below) at the expense of ripple in the passband. Chebyshev filters can be designed with passband ripples from 0.01 to 3dB but the range 0.1 to 1dB is most useful. Bandwidths (ω_c) are quoted at either the equiripple point entering the stopband or at the −3dB point. This is an item to watch out for, when using filter tables from different sources, to prevent inaccuracies in the final filter design. The tables of lowpass pole positions given here are normalised to 1 ohm and 1 rad/second at the −3dB point.

Figure 4.46 and 4.47 show the group delay and transient response respectively of Chebyshev 0.5dB ripple filters and these are clearly worse than those for Butterworth or Bessel (see below).

Fig. 4.46 Group-delay characteristics for Chebyshev filters with 0.5–dB ripple.

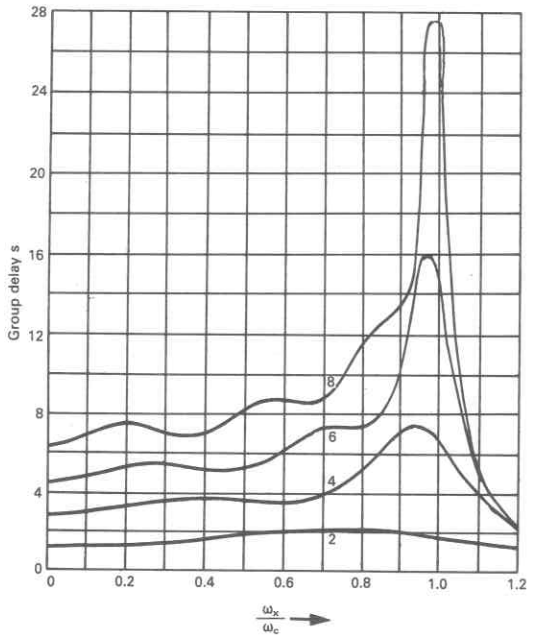
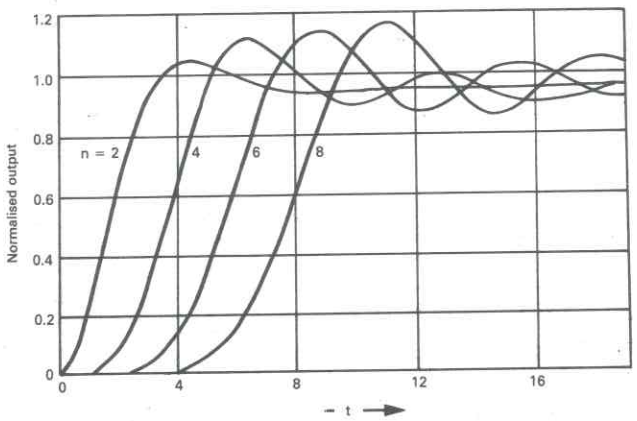


Fig. 4.47 Step response for Chebyshev filters with 0.5–dB ripple.



The order of filter n required for slope factor ω_s/ω_c at attenuation Hs and passband ripple 0.5 and 1 dB can be determined from Figure 4.48 (a) & (b). The pole positions for these filters are given in Table 4.3.

Table 4.3 Chebyschev pole locations.

	0.5–dB Chebyshev Pole Locations		1–dB Chebyshev Pole Locations	
Order n	Real Part $-\alpha$	Imaginary Part $\pm j\beta$	Real Part $-\alpha$	Imaginary Part $\pm j\beta$
2	0.5129	0.7225	0.4508	0.7351
3	0.2683 0.5366	0.8753	0.2257 0.4513	0.8822
4	0.3872 0.1605	0.3850 0.9297	0.3199 0.1325	0.3868 0.9339
5	0.2767 0.1057 0.3420	0.5902 0.9550	0.2265 0.08652 0.2800	0.5918 0.9575
6	0.2784 0.2307 0.07459	0.2596 0.7091 0.9687	0.2268 0.1660 0.06076	0.2601 0.7106 0.9707
7	0.2241 0.1550 0.05534 0.2487	0.4349 0.7836 0.9771	0.1819 0.1259 0.04494 0.2019	0.4354 0.7846 0.9785
8	0.2144 0.1817 0.1214 0.04264	0.1955 0.5565 0.8328 0.9824	0.1737 0.1473 0.09840 0.03456	0.1956 0.5571 0.8337 0.9836

normalised to 1 ohm & 1 rad/sec at −3dB

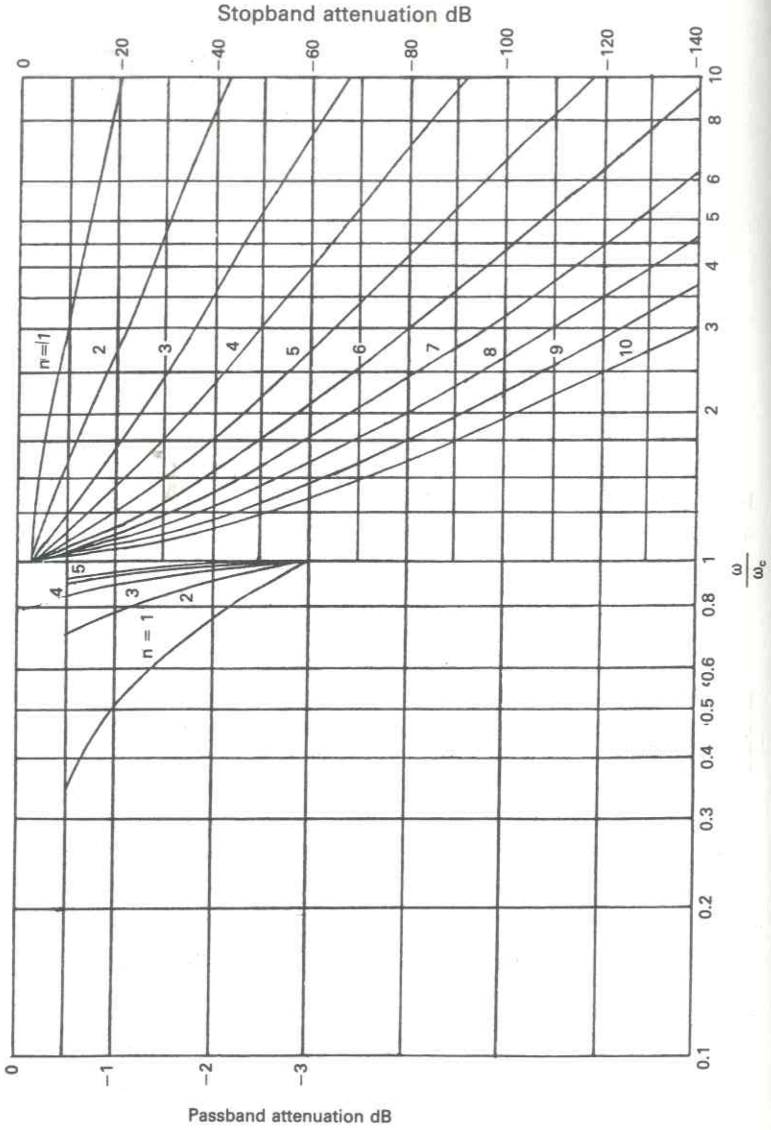


Fig. 4.48(a) Chebyshev attenuation characteristic with 0.5dB ripple.

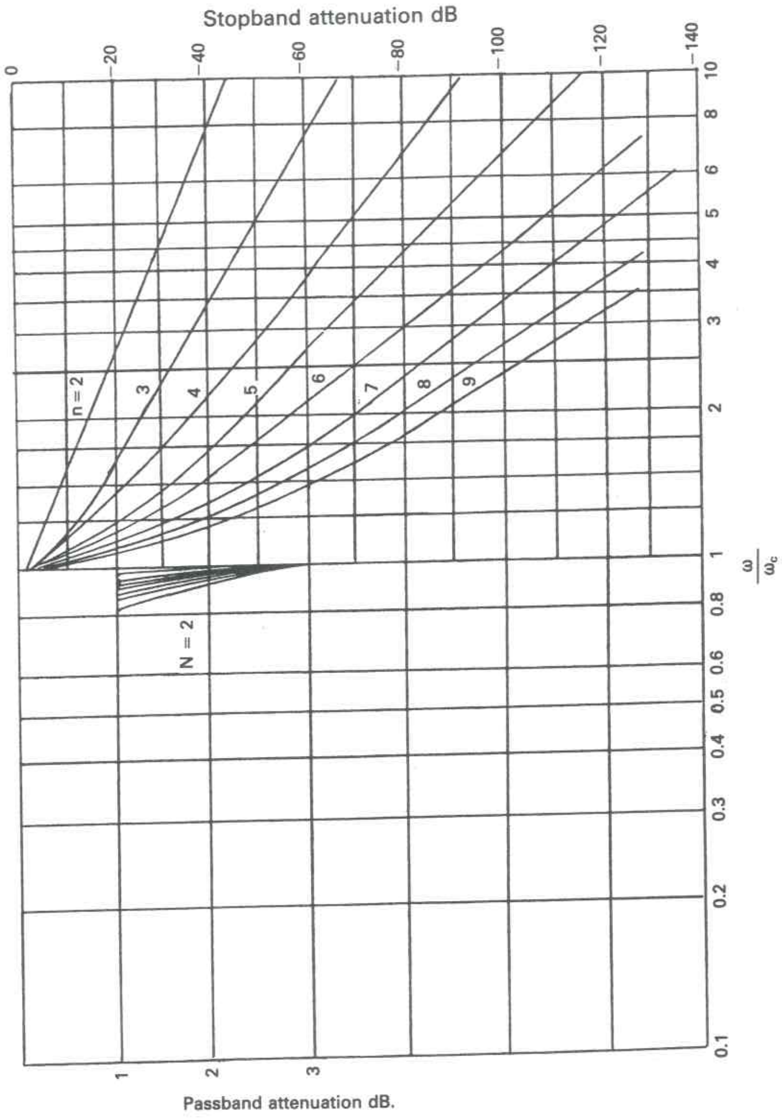
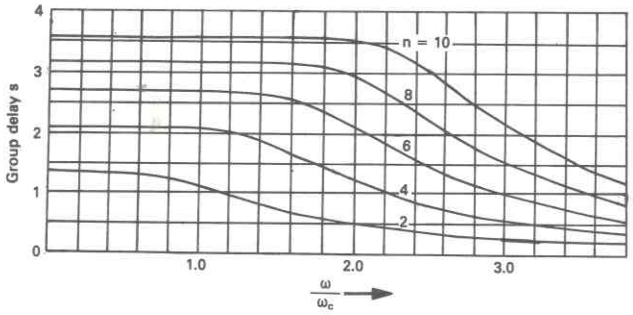


Fig. 4.48(b) Chebyshev attenuation characteristic with 1dB ripple.

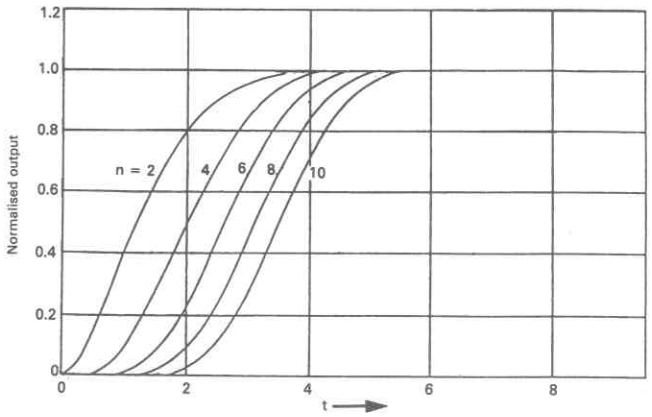
Bessel-Maximally Flat Delay

The Bessel transfer function has been optimised to obtain a maximally flat delay; that is, it has a linear phase response. The step response shows negligible overshoot and thus these filters pass transient waveforms with the minimum distortion. The amplitude response however is much less selective than the other types. Increasing the order of the filter does not improve the selectivity around cut-off but extends the region of flat delay into the stopband. Bessel filters are for use where transient properties are of major importance.

Fig. 4.49 Group-delay characteristics for maximally flat delay (Bessel) filters.



4.50 Step response for maximally flat delay (Bessel) filters.

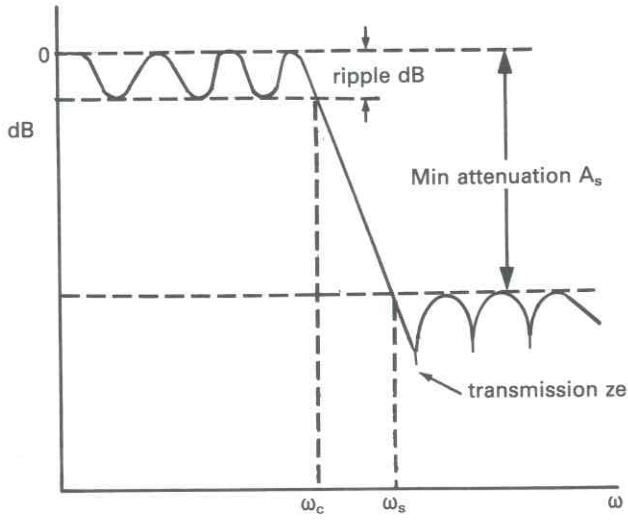


Figures 4.49 and 4.50 give the group delay and transient responses respectively. The order of filter required for shape factor ω_s/ω_c at attenuation Hs can be determined from Figure 4.51 and the pole positions are given in Table 4.2(b).

Elliptic (Cauer)-Function

Elliptic function filters feature stopband transmission zeros and have the sharpest roll-off characteristics for a given number of poles. Improved roll-off performance is obtained at the expense of return lobes in the stopband Figure 4.52.

Fig. 4.52 Typical elliptic-function low-pass filter response.



The circuit realizations for Elliptic function filters are more complex than the others and due to the higher Q's required suffer from greater sensitivity to component tolerances. It is suggested that the reader consult references 4 and 5 for detailed information.

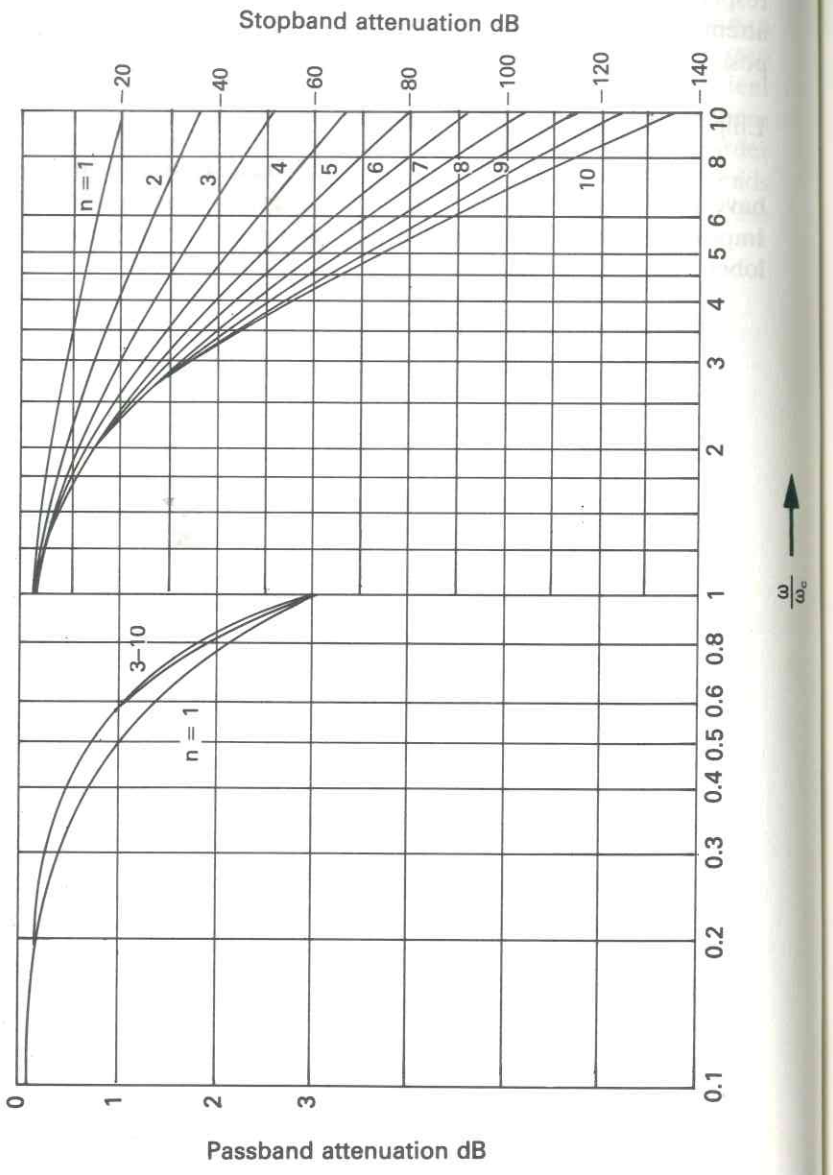


Fig. 4.51 Bessel attenuation characteristic.

Realisation of Filter Transfer Functions

Filter Section Transfer Functions

To realise the above filter transfer function responses circuit topologies have to be used that can position the poles and zeros of the function correctly. These can be expressed directly in terms of pole or zero positions $-\alpha \pm j\beta$ but are more usually expressed in terms of damping d (or it's inverse $Q = 1/d$ for bandpass) and resonant frequency ω_o. The standard network transfer functions for a two pole ($n = 2$) lowpass highpass and bandpass are given below:

$$\text{Lowpass } H(s) = \frac{H_o\omega_o^2}{s^2 + d\omega_o s + \omega_o^2}$$

where H_o = Amplitude const.
ω_o = cut-off freq.
s = complex variable.

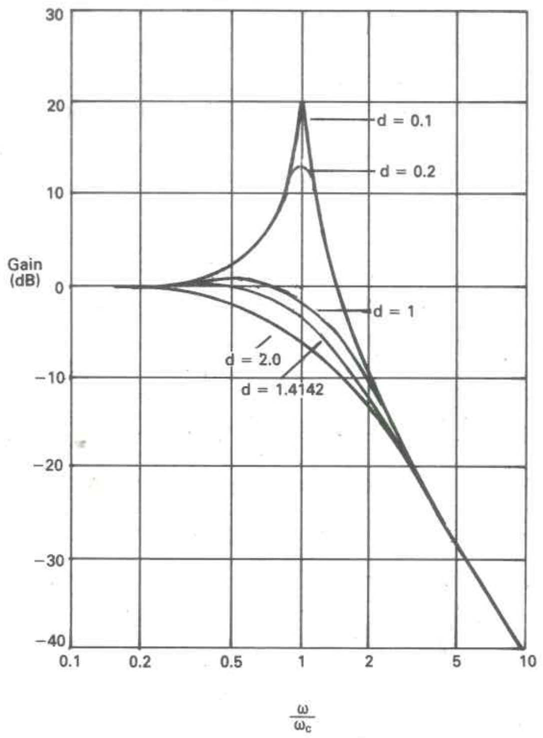
$$\text{Highpass } H(s) = \frac{H_o s^2}{s^2 + d\omega_o s + \omega_o^2}$$

$$\text{Bandpass } H(s) = \frac{H_o s\omega_o}{s^2 + (\omega_o/Q)s + \omega_o^2}$$

The poles of the above equations describe the basic filter shape and the zeros perform the transformation of a lowpass function into highpass or bandpass response respectively. (The relationship between the pole positions and d and ω_o will be described below.) It is important to draw a distinction between a filter section transfer function and the overall filter transfer function. For lowpass and highpass these are the same but for bandpass filters each two pole (2nd order) filter section contributes only one pole to the final bandpass filter response. A distinction may also exist between the cut-off frequency of the filter (ω_c) and the cut-off frequency of the individual sections (ω_o). For example for a Butterworth filter the cut-off frequencies for each section are identical but for Chebyshev they are staggered to get the overall filter response. Thus to design a filter to a given response shape the values of d (or 1/Q) and ω_o for each section have to be set.

Figure 4.53 shows how the amplitude response of a lowpass two pole section varies with change of damping d. Frequency ω_o is adjusted to position this amplitude response.

Fig. 4.53 Normalised amplitude response Vs. damping d for 2nd order lowpass filter.



In summary an overall filter response shape is manipulated by the adjustment of the individual 2nd order filter sections damping d and resonant frequency ω_o.

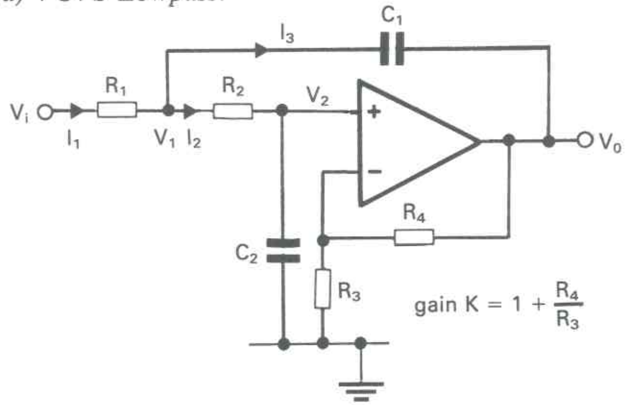
Filter Circuit Topologies

Voltage Controlled Voltage Source (VCVS)

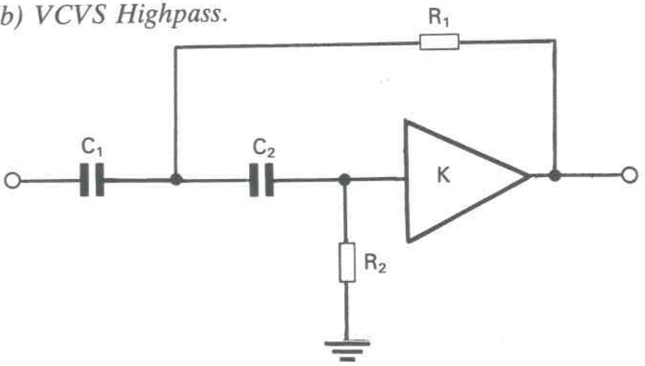
Otherwise known as Sallen and Key circuits these use a positive gain K and as shown by Figure 4.54 can be used to implement all types of filters.

Fig. 4.54

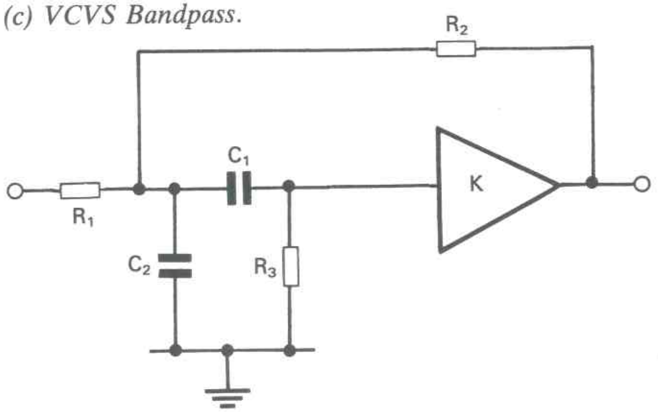
(a) VCVS Lowpass.



(b) VCVS Highpass.



(c) VCVS Bandpass.



They are most successful with low and highpass filters of damping > 0.5. An example of the transfer function derivation of Figure 4.54(a) is shown below.

$$I_1 = \frac{V_{in} - V_1}{R_1} = I_2 + I_3 = \frac{V_1 - V_2}{R_2} + (V_1 - KV_2)sC_1$$

$V_1 = V_2(1 + R_2C_2S)$ and $V_{out} = KV_2$ re-arranging these:

$$\frac{V_{out}}{R_{in}} = \frac{K\times 1/(R_1R_2C_1C_2)}{s^2 + [1/R_1C_1 + 1/R_2C_1 + (1-K)/R_2C_2]s + 1/(R_1R_2C_1C_2)}$$

Thus $d.\omega_o = [1/R_1C_1 + 1/R_2C_1 + (1-K)/R_2C_2]$

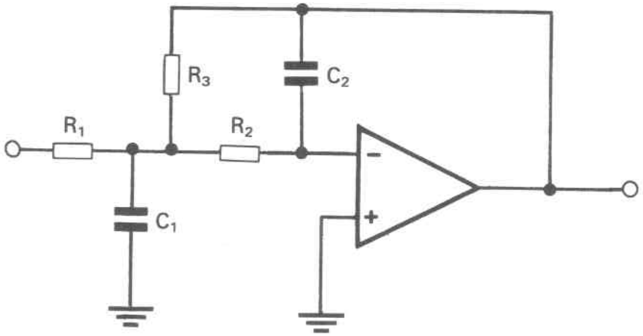
and $\omega_o^2 = 1/R_1R_2C_1C_2$

As will be shown below some simplifying assumptions can be made to make filter design easier.

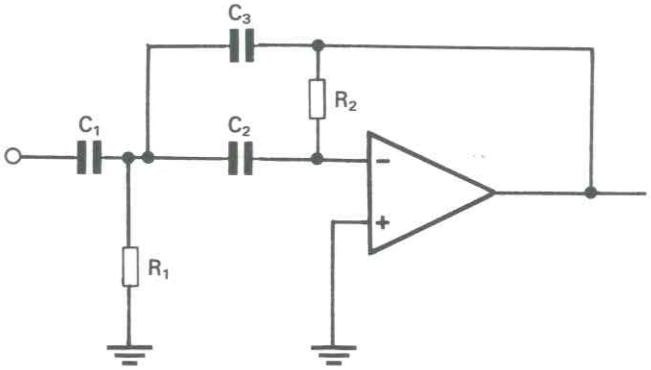
Infinite Gain Multiple Feedback (MFB) Circuits

Fig. 4.55 Multiple feedback (MFB) filters.

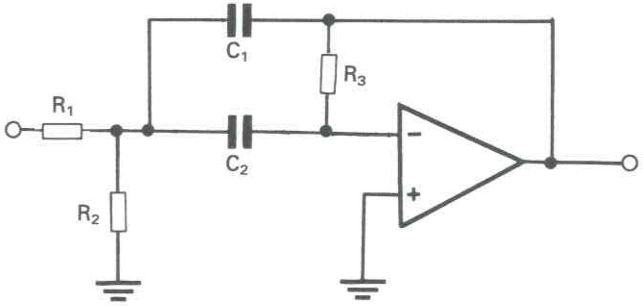
(a) MFB lowpass.



(b) MFB highpass



(c) MFB Bandpass.



Configurations for each type of filter are shown in Figure 4.55. The MFB circuit is most popularly used for bandpass filters with Q's <5, the transfer function of this (Figure 4.55(c)) is:

$$\frac{V_{out}}{V_{in}} = \frac{-s(1/R_1C_1)}{s^2 + s(1/R_3)(1/C_1 + 1/C_2) + (1/R_3C_1C_2)(1/R_1 + 1/R_2)}$$

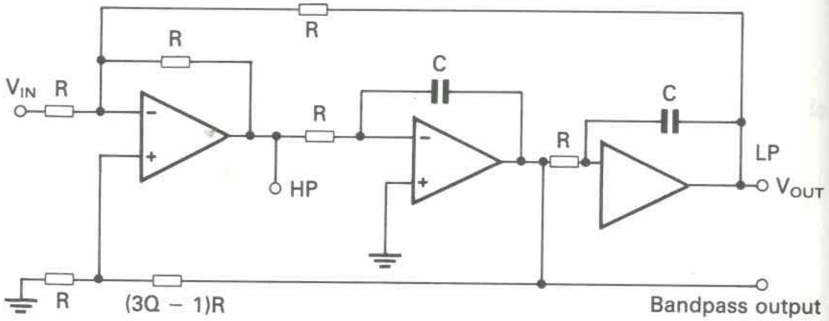
$$\frac{\omega_o}{Q} = (1/R_3)(1/C_1 + 1/C_2)\ \&\ \omega_o^2 = (1/R_3C_1C_2)(1/R_1 + 1/R_2)$$

State Variable Circuit

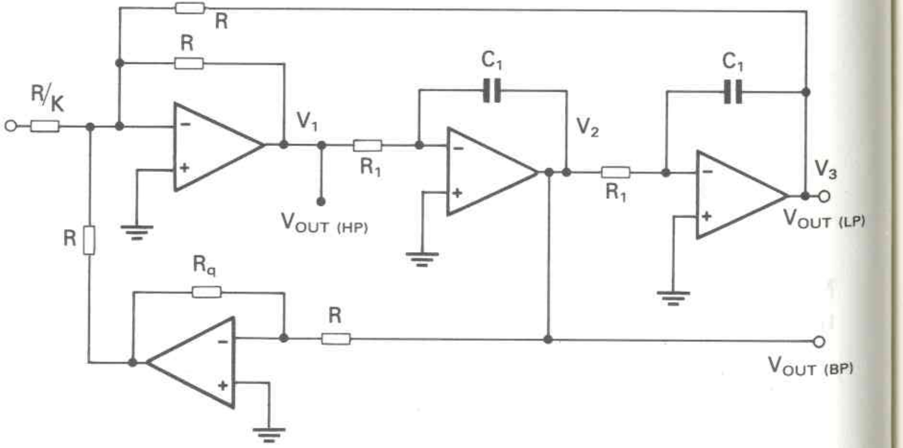
The state variable filter uses integrators and amplifiers to construct an analogue computer model of the basic filter transfer functions. The circuit realises all the two pole filter types but is most useful as a bandpass filter as it is able to operate with high Q values <500. It is less efficient in the use of op-amps for lowpass and highpass circuits, which have low Q's (<1.5), and can successfully be built with single op-amp circuits. Figure 4.56 gives two variations of the circuit.

4.56 State variable filters.

(a) Gain fixed at + Q.



(b) Variable gain at KQ.



Analysing the circuit of Figure 4.56(b) gives:

$$V_1 = -\left(K.V_{in} - V_2.\frac{R_q}{R} + V_3\right) \quad \text{.........................} \quad (1)$$

$$V_2 = -\frac{V_1}{sR_1C_1} \quad \text{...} \quad (2)$$

$$V_3 = -\frac{V_2}{sR_1C_1} \quad \text{...} \quad (3)$$

substituting in (2) for a bandpass response gives:

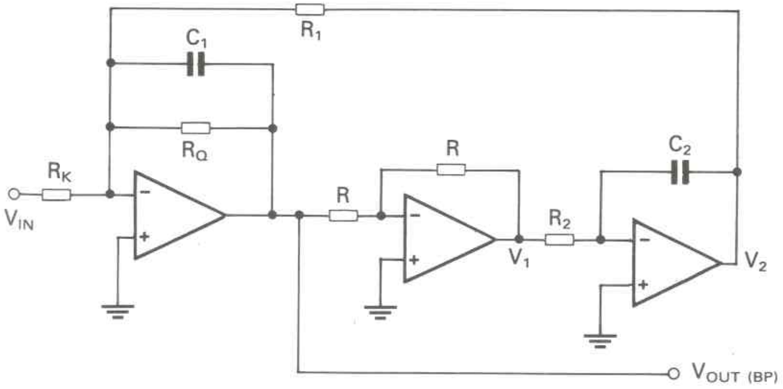
$$\frac{V_{out}\ (BP)}{V_{in}} = \frac{-K \times s(1/R_1C_1)}{s^2 + s(R_q/R)(1/R_1C_1) + 1/(R_1C_1)^2}$$

Transfer functions for lowpass and highpass can be similarly generated from equations (1) to (3).

Biquad

This is a circuit that realises a bandpass filter, but has a poor lowpass performance and no highpass output at all. It has at first sight a resemblance to the State Variable Filter but is actually different as the damping is applied by means of a resistor across the first integrator.

Fig. 4.57 Biquad bandpass filter.



The analysis of the circuit shown in Figure 4.57 is given below:

$$C_1 \text{ in parallel with } R_Q = \frac{R_Q}{1 + sC_1R_Q} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$V_2 = V_{out} \cdot \frac{1}{sC_2R_2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

$$V_{out} = -\left(V_{in} \times \frac{R_Q}{R_K(1 + sC_1R_Q)} + V_2 \times \frac{R_Q}{R_1(1 + sC_1R_Q)}\right)$$

$$. \ (3)$$

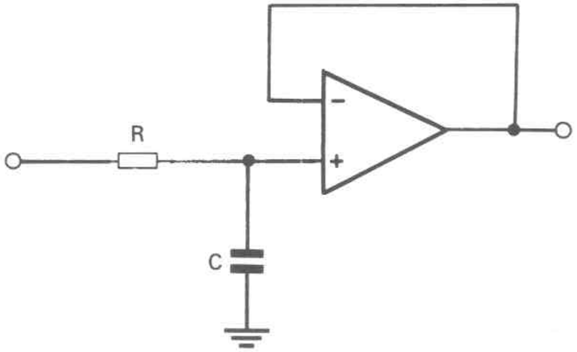
Substituting for V_2 and re-arranging:

$$V_{out} = -\frac{R_Q}{R_K} \times \frac{s(1/C_1R_Q)}{s^2 + s(1/C_1R_Q) + (1/R_1R_2C_1C_2)}$$

thus $\omega_o{}^2 = (1/R_1R_2C_1C_2)$ and $\omega_o/Q = (1/C_1R_Q)$.

In summary all these circuit topologies assume that the source impedance is low and provides, where necessary, the appropriate level of d.c. bias. This is most effectively achieved by use of a suitable biased voltage follower to buffer the filter input. A simple RC voltage divider may be used at the input of the voltage follower to produce an odd order filter section with $\omega_o = (1/RC)$. (See Figure 4.58).

Fig. 4.58 Odd order filter section.



Filter Normalization and Scaling

The filter Tables 4.2 and 4.3 give pole positions that produce filters normalised to 1 ohm and 1 radian/second with cut-off at −3dB. To produce a usable filter these values have to be scaled for impedance Z and frequency ω_c. To scale a filter to impedance Z all resistor values are multipled by Z and all capacitor values are divided by Z (i.e. $ZX_c = (Z \times 1/(\omega C) = 1/(\omega C/Z)$; this assumes a normalised impedance of 1 ohm. Where a filter already is at impedance z the factor is Z/z. To scale a filter to frequency f_c all capacitor values are divided by $2\pi f_c$ (which equals ω_c the cut-off frequency of the whole filter); this gives a smaller value of capacitor with the same impedance at a higher frequency.

Cascaded Sections

The basic building blocks of single and two pole filter sections are cascaded to form higher orders of filter. Greatest input signal dynamic range and prevention against op-amp saturation by high amplitude signals, particularly at the band edge, is achieved by cascading sections in order of decreasing damping (increasing Q) with the first section having the highest damping (lowest Q).

Op-amp Effects on Filter Performance

Gain-bandwidth and slew rate will limit the accuracy and highest frequency of operation for a given filter realisation. As the filter gain-cut-off frequency product approaches the op-amp gain-bandwidth product the accuracy of the cut-off frequency will be reduced. Closed loop phase shift under similar conditions will cause Q enhancement. To limit these effects open loop gain over closed loop gain should be >10 at the filters cut-off frequency. For filters made from integrators the open loop gain should be >5×Q.

Slew-rate limits the large signal bandwidth, but more subtly it can effect stability with increasing amplitude. This is due to additional phase shift being introduced when the signal is close to the slew limit.

These considerations should be taken into account when choosing the bias mode of a LinCMOS op-amp for a particular filter specification.

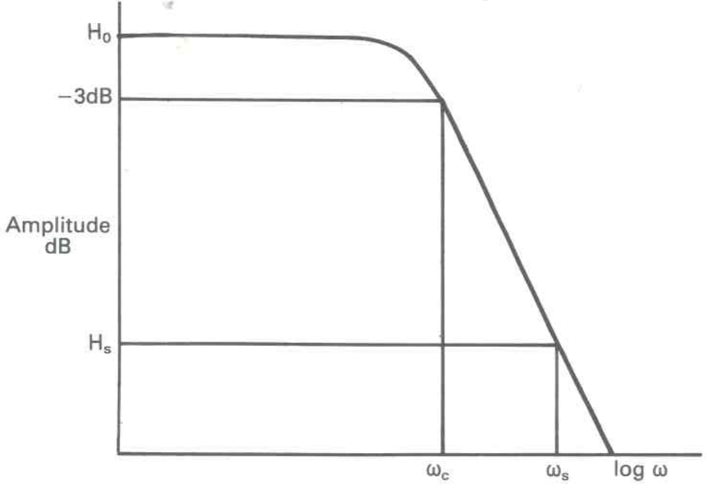
Filter Design Examples

General Design Steps

1. Determine the most important filter characteristic required in terms of amplitude, group delay (phase linearity) or transient response. Choose the most appropriate filter transfer function or by default use the Butterworth response as this gives the best overall compromise.

2. Determine the order n of the filter required in terms of the lowpass response. Figure 4.59 shows slope factor ω_s/ω_c at attenuation H_s. This can be used directly in the above equation (page 4–37) for Butterworth or from Figures 4.48 or 4.51 for Chebyschev or Bessel.

Fig. 4.59 Determination of slope factor $\frac{\omega_s}{\omega_c}$ *at attenuation* H_s.



3. Determine the number of sections needed to implement the filter. Each 2nd order section gives order n = 2 for low or highpass filters and order n = 1 for bandpass filters.

4. Determine the d (or Q) and ω_o for each section from the poles positions of Table 4.2 or 4.3.

5. Determine the circuit topology to be used taking d or Q values and sensitivities into account. VCVS are the first choice for lowpass and highpass filters (low Q). For bandpass filters MFB are used for low Q <5 and state variable for higher value Q's.

6. Translate d or Q and ω_o values into circuit component values by comparing the standard filter transfer function with the chosen circuit transfer function and making simplifications where possible. The most general of these is to equate all R's and C's.

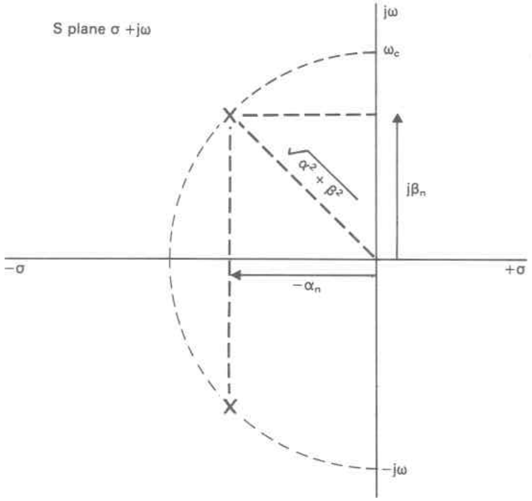
7. Scale the normalised 1 ohm and 1 radian/second values for the operating impedance and −3dB cut-off frequency ω_c. The choice of impedance may be implied by starting with standard value capacitors (see example below).

Lowpass Filter Design Examples

Determination of d and ωo from pole positions

The arrangement of pole positions $\alpha_n \pm j\beta_n$ (Figure 4.60) determines a filters frequency and phase response.

Fig. 4.60 Pole–zero diagram for 2nd order lowpass section.



Damping d or 1/Q and ω_o can be determined in terms of these as shown below:

Filter section two pole response can be expressed in terms of overall filter cut-off frequency ω_c, where coefficients a_0 & a_1 modify these for filter sections:

$$H(s) = \frac{a_0\omega_c^2}{s^2 + sa_1\omega_c + a_0\omega_c^2} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

In terms of pole positions:

$$= \frac{s_1s_2}{(s - s_1)(s - s_2)} = \frac{s_1s_2}{s^2 - (s_1 + s_2)s + s_1s_2}$$

where $s_1 = -\alpha + j\beta$ and $s_2 = -\alpha - j\beta$

$$\therefore H(s) = \frac{(\alpha^2 + \beta^2)\omega_c^2}{s^2 + 2\alpha\omega_c s + (\alpha^2 + \beta^2)\omega_c^2} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

Using the standard form in terms of d or 1/Q and ω_o (where ω_o is the filter section cut-off):

$$H(s) = \frac{\omega_o^2}{s^2 + d\omega_o s + \omega_o^2} \quad \ldots\ldots\ldots\ldots\ldots (3)$$

equating terms of (3) with (1).

$$\omega_o^2 = a_0\omega_c^2 \ \&\ d\omega_o = a_1\omega_c$$

Then $\omega_o = \sqrt{a_0} \times \omega_c$ and $d = \frac{a_1}{\sqrt{a_0}}$

by comparing (1) with (2) $\sqrt{a_0} = \sqrt{(\alpha^2 + \beta^2)}$

$$\&\ \therefore d = \frac{2\alpha}{\sqrt{(\alpha^2 + \beta^2)}} \quad \ldots\ldots\ldots\ldots\ldots (A)$$

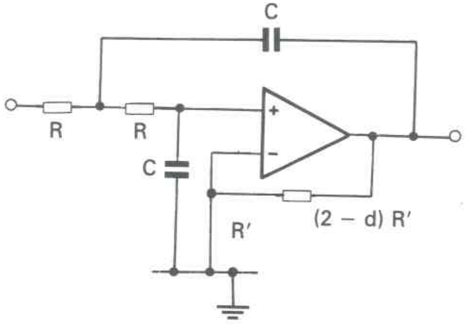
For ω_c normalised at 1 radian/second $\omega_o = \sqrt{(\alpha^2 + \beta^2)}$ .... (B)

Lowpass VCVS

$$d\omega_o = [1/R_1C_1 + 1/R_2C_1 + (1 - K)/R_2C_2] \ \&\ \omega_o^2 = 1/R_1R_2C_1C_2$$

Figure 4.61 gives equal component case $R_1 = R_2 = R$; $C_1 = C_2 = C$ $d\omega_o = (3 - K)/RC$; $\omega_o = 1/RC$; $\therefore d = (3 - K)$ giving gain setting resistors R′ and R′ (2 − d).

Fig. 4.61 Equal-component VCVS lowpass filter.



A Butterworth filter 2nd order (n = 2) has $\alpha = -0.7071$, $\beta = \pm 0.7071$ from Table 4.2. The above equations (A) & (B) gives $\omega_o = 1$ and $d = 1.4142$.

With a filter specification of $f_c = 1$ kHz and impedance Z = 10kohms. An attenuation of 24dB exists at 4kHz (calculated from the Butterworth attenuation equation page 4–37). Scaling for impedance and frequency using $\omega_o = 1/R_n.C_n$ (where suffix n indicates values normalised to 1 ohm and 1 rad/sec), for some chosen value of capacitor C then:

$$C = C_n \times \frac{1}{\omega_c Z} = C_n \times \frac{1}{2\pi \times 10^3 \times 10^4} = C_n \times 15.9 \times 10^{-9}$$

choose C = 2.2nF $\therefore C_n = 2.2/15.9 = 0.1382$

$R_n = \omega_o/C_n = 1/0.1382 = 7.234$ and scaled to 10 kohms = 72.34 kohms. This result can be achieved directly from

$$R_n = \frac{1}{\omega_o C_n}; C = \frac{C_n}{\omega_c Z} \quad \text{gives } R = [R_n Z] = \frac{1}{\omega_o\omega_c C}$$

where R is the resistor value resulting from choosing C. Normalised filter section cut-off frequency ω_o is seen to be a scaling factor for actual filter-cut-off frequency ω_c.

Gain setting resistors (referring to Figure 4.61): R′ & R′ (2 − d) = R′ (0.5858) giving typical values of 200k and 117.2kohm (120k).

Tuning the equal component VCVS is achieved by varying R_1 & R_2 (=R) or C_1 & C_2 (=C) together.

Chebyshev Equal Component VCVS

Filter specification: f_c = 1kHz attenuation >20dB at 3.5kHz and <1.5 dB at 800Hz.

The slope factor $\omega_s/\omega_c = 3.5$, from Figure 4.48(b) of Chebyshev filters with 1dB ripple, order n = 2 will fulfil this requirement. Damping d and ω_o are calculated from the pole positions of Table 4.3 using equations (A) & (B): d = 1.0455 and $\omega_o = 0.8623$. If C is chosen as above to be 2.2nF then $R = 1/(\omega_o\omega_c C)$ = 83.9 kohms. Gain setting resistors R′ & R′ (2 − d) = 0.9545R′ typically both 100k's for practical purposes.

For higher orders of filter the process is repeated for each section. Suitable values of capacitor or impedance are chosen independently for each section.

Chebyshev VCVS Fourth Order

Filter specification: f_c = 1kHz, attenuation >60dB at 4kHz and <1dB at 800Hz. From Figure 4.48(b) of 1dB responses a 4th order is seen to fulfil this requirement, as ω_s/ω_c = 0.8 and 4. Two 2nd order sections are needed to realise this filter with $d_1 = 1.2746$, $\omega_{o1} = 0.50195$ and $d_2 = 0.28094$, $\omega_{o2} = 0.94325$ calculated using equations A & B from the pole positions Table 4.3.

Using the equal component VCVS circuit: scaling for impedance by reason of the value of capacitor chosen (that is choosing $C = C_1 = C_2$ = 2.2nF) and scaling for frequency $2\pi f_c$:

$$R_1 = \frac{1}{\omega_c\omega_o C} = 144\text{kohms (150k) similarly } R_2 = 76.7\text{kohms (75k)}$$

Gain setting resistors R_1' & R_1' (2 − d) = R_1' (0.7254) (typ 200k & 150k).

Gain setting resistors R_2' & R_2' (2 − d) = R_2' (1.7190) (typ 130k & 220k).

Bessel VCVS Fourth Order

Bessel filters can be used to provide a constant delay to a signal. As can be seen from Figure 4.49 for n = 4 a flat delay extends up to the cut-off frequency. From the pole positions of Table 4.2(b) $d_1 = 1.91595$, $\omega_{o1} = 1.41924$ and $d_2 = 1.2415$, $\omega_{o2} = 1.591124$ using equations (A) & (B). Then for the equal component VCVS again choosing C = 2.2nF, R_1 = 51kohm R_1' (2 − d) = R_1' (0.084) (100k & 8.2k), R_2 = 47kohm R_2' (2 − d) = R_2' (0.7852) (100k & 75k).

Unity Gain VCVS

Another popular simplification of the lowpass VCVS transfer function is to make K = 1 i.e. unity gain. (This gives a filter with the widest possible bandwidth).

$$\text{Thus } d\omega_o = \frac{1}{R_1C_1} = \frac{1}{R_2C_1}$$

$$\text{putting } R_1 = R_2 = R; \quad d\omega_o = \frac{2}{RC_1}$$

$$\text{and } \omega_o^2 = \frac{1}{R_1R_2C_1C_2} = \frac{1}{R^2C_1C_2};$$

$$\text{thus } C_1 = \frac{2}{Rd\omega_o} \;\&\; C_2 = \frac{d}{2R\omega_o}$$

$$\& \frac{C_1}{C_2} = \left(\frac{2}{d}\right)^2$$

e.g. for a 2nd order Butterworth Filter d = 1.4142 & $\omega_o = 1$ choose C_2 = 2.2nF $C_1 = C_2(2/d)^2 = 2$ ∴ C_1 = 4.4nF.

Impedance scaling (by capacitance choice) and frequency scaling to f_c = 1kHz $R = 1/(\omega_o\omega_c dC_1)$ = 51kohms.

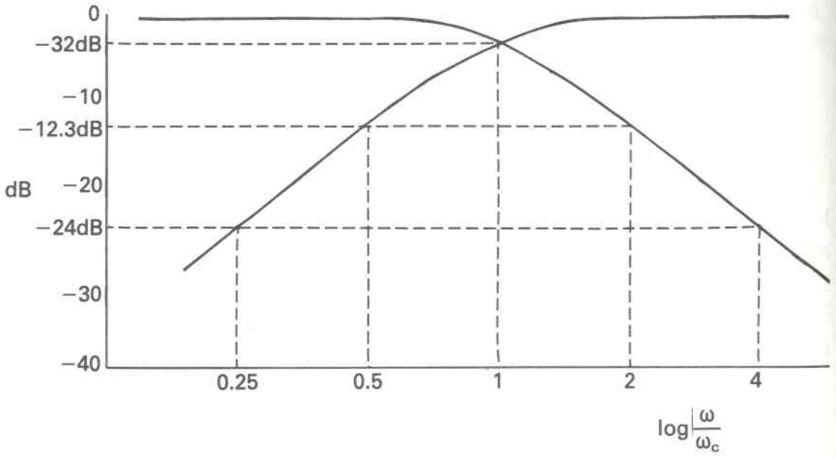
This circuit can be tuned by varying R_1 & R_2 together and by varying C_1 & C_2 if their ratio $(d/2)^2$ is maintained.

Other unity gain ($K = 1$) simplifications such as: a) $C_1 = C_2 = C$ & b) $R_1.C_1 = R_2C_2$ i.e. $a = C_1/C_2 = R_2/R_1$ yield complex interdependence between circuit variables and complicated tuning.

Highpass Filters

With the proviso that a true active highpass filter cannot be produced because finite op-amp gain-bandwidth limits the high frequency performance, designing such a filter is a relatively straight forward matter. It is achieved by transposing a highpass into a lowpass design by replacing normalised frequencies f of the highpass requirement into normalised frequencies l/f of a lowpass 'prototype' (see Figure 4.62). A lowpass filter is thus designed and then components (R's & C's) for a typical VCVS topology are then interchanged to give the highpass filter.

Fig. 4.62 Typical normalised highpass – lowpass transformation.



Using the lowpass Butterworth n = 2 (page 4–57) example above, ω_s/ω_c at −24dB = 4, this is equivalent to $\omega_s/\omega_c = 0.25$ (250Hz for f_c = 1kHz) for the highpass transposition. Thus a highpass filter with f_c = 1kHz and −24dB at 250Hz is produced by putting the lowpass circuit values in the circuit configuration of Figure 4.54(b).

To achieve the widest bandwidth the unity gain VCVS configuration should be used along with the high bias mode LinCMOS op-amps. Wide bandwidth bandpass filters that are made up of cascaded lowpass and highpass sections give one of the best uses of this type of high pass filter.

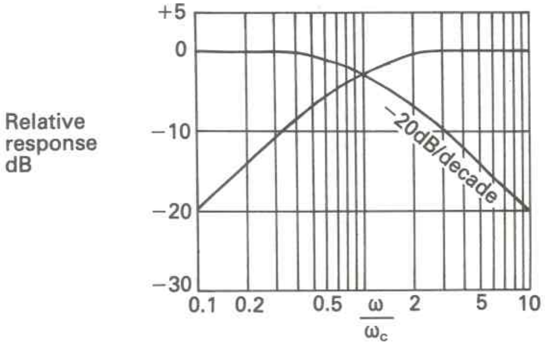
Bandpass Filters Design Examples

Introduction

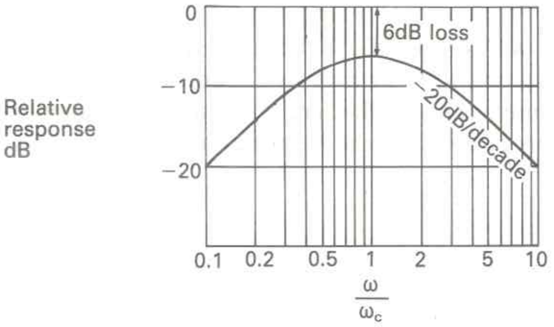
Bandpass filters can be divided into two types distinguished by the ratio of upper (f_U) to lower (f_L) −3dB cut-off frequency. When this ratio exceeds approximately 2 (an octave) the filter is a wideband type and is implemented by cascading highpass and lowpass sections. The criteria for wideband filters can also be expressed in terms of centre frequency f_r $(= \sqrt{f_U f_L})$ and bandwidth ($BW = f_U - f_L$) where $BW/f_r \leqslant 0.7$ (= 1/Q for a single 2 pole section). Figure 4.63 gives a comparison between wideband and narrowband for $f_U/f_L < 2$, showing a loss for wideband and Q magnification for narrowband.

Fig. 4.63 Wideband filter limitations.

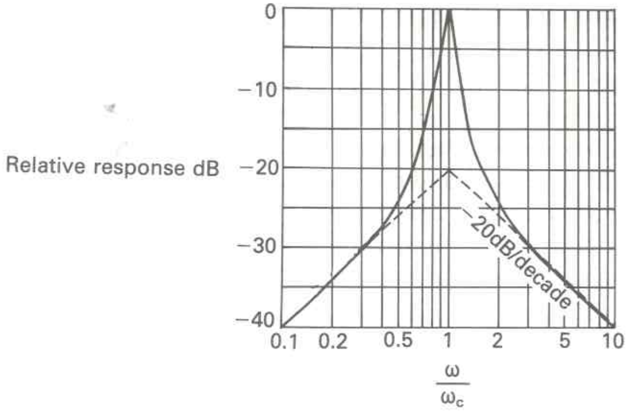
(a) Individual low & highpass responses.



(b) *Sum of low & highpass responses showing loss.*



(c) *Narrow band single pole response with* $Q = 10$.



For ratios of f_U/f_L less than an octave narrowband filter sections are used that realise bandpass transfer functions directly.

The response shapes for bandpass filters are obtained by transforming lowpass transfer functions into bandpass types and then implemented by cascading bandpass filter sections.

Lowpass to Bandpass Transformation

The bandpass response is transformed from the lowpass response as follows:

The normalised lowpass transfer function $H(s) = \frac{1}{S+1}$

is transformed into bandpass by substitution of:

$$S = \frac{1}{BW}\left(\frac{s^2 + \omega_r^2}{s}\right) \text{ to give:}$$

$$H(s) = \frac{s\omega_r/Q}{s^2 + s\omega_r/Q + \omega_r^2}$$

Where $Q = \frac{\omega}{BW}$ and ω is the centre frequency.

(S and s are both complex variables.)

(ω_r is used here to differentiate from ω_c and ω_o, the low and highpass overall filter and section −3dB cut-off frequencies respectively.)

This transformation can be described in terms of a pole-zero diagram, as shown in Figure 4.64, where a single low frequency pole is transformed to give a pair of conjugate poles and a zero at the origin. The transformation above, by definition, transforms the lowpass bandwidth ω_c into the bandpass bandwidth as shown.

Fig. 4.64 Single pole lowpass to bandpass transformation.

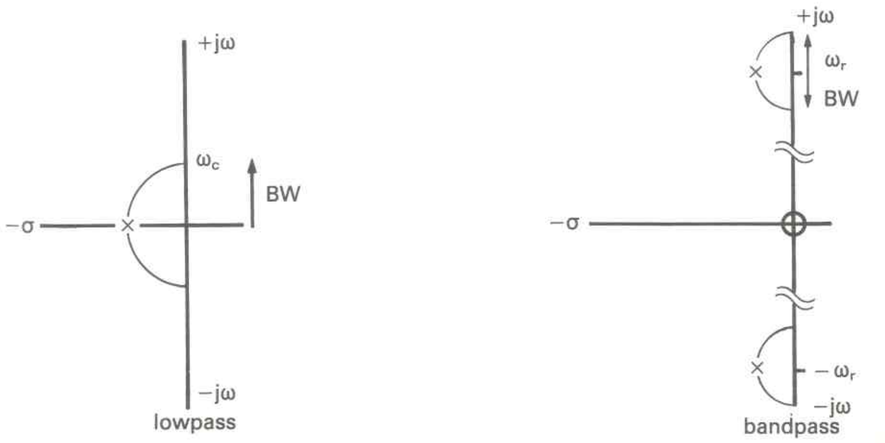


Figure 4.65 show this transformation for a multi-pole response and Figure 4.66 shows the same in terms of filter amplitude response.

Fig. 4.65 Multiple lowpass to bandpass transformation.

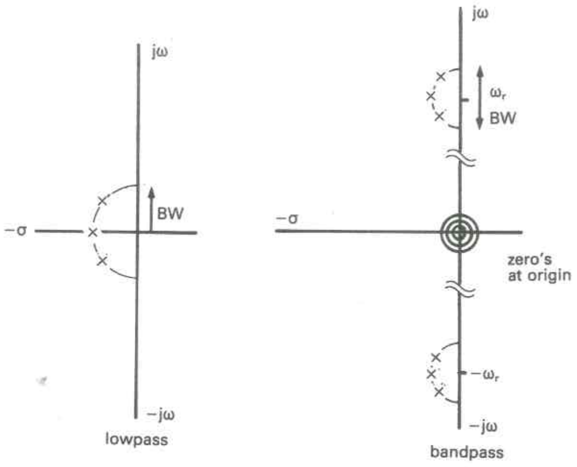
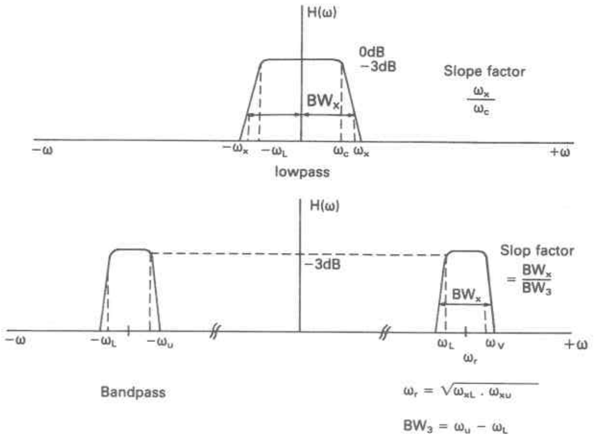


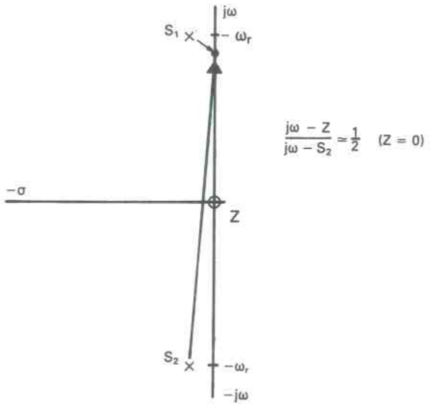
Fig. 4.66 Lowpass to bandpass transformation shown in terms of frequency response.



Narrowband Approximation

To obtain the amplitude and phase response from the diagrams of Figures 4.64 and 4.65 all the poles and zeros have to be taken into consideration. With increasing values of Q the poles move closer to the jω axis. Using this fact, an approximation can be made so that only the cluster of poles around ω_r need be considered for moderate and high values of Q. Values of $Q>5$ give reasonable and increasing accuracy. For lower values some distortion of the amplitude response will result and empirical adjustment may be necessary to obtain the desired response.

Fig. 4.67 Pole – zero diagram showing narrowband approximation.


jω
S_1
ω_r
$\frac{j\omega - Z}{j\omega - S_2} \simeq \frac{1}{2}$ (Z = 0)
−σ
Z
S_2
$-\omega_r$
−jω

The bandpass response expressed in terms of poles and zeros is given by:

$$H(s) = \frac{\omega_r}{Q} \times \frac{s}{(s - s_1)(s - s_2)}$$

The substitution s = jω can be made for operation along the frequency axis.

$$H(j\omega) = \frac{\omega_r}{Q} \times \frac{j\omega}{(j\omega - s_1)(j\omega - s_2)}$$

Reference to Figure 4.67 shows that when $j\omega \simeq j\omega_r$

$$\frac{j\omega}{j\omega - s_2} \simeq \frac{1}{2} \text{ and } H(j\omega) = \frac{\omega_r}{Q} \times \frac{1}{(j\omega - s_1)} \text{ centred on } \omega_r.$$

This shows that a bandpass 2 pole (2nd order) section contributes only one pole (order) to an overall bandpass response. It also shows that lowpass poles clustered around the origin can be used to determine a new set of poles with a bandpass response. These new poles will give a bandpass bandwidth BW equal to the cut-off frequency ω_c of the lowpass poles and be centred on ω_r.

Lowpass to Bandpass pole position Transformation

Fig. 4.68 Second-order lowpass pole positions.

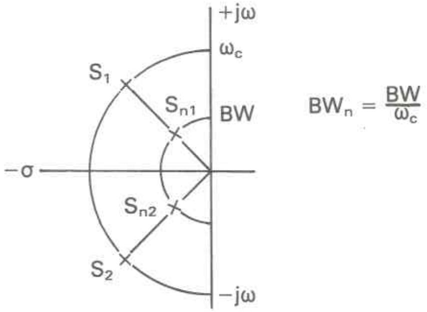
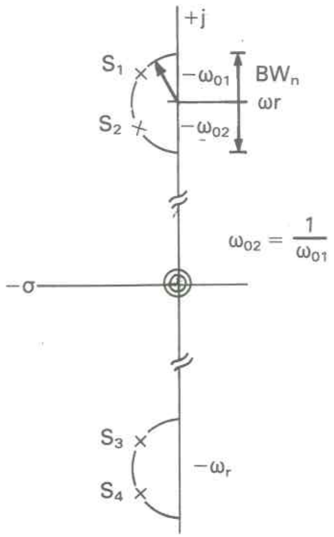


Figure 4.68 is a typical pole-zero diagram for a symmetrical pair of poles describing a 2nd order lowpass filter with cut-off ω_c. The positions of the poles $s_{1,2} = -\alpha \pm j\beta$ are proportional to the cut-off frequency ω_c. If an arbitrary cut-off called bandwidth BW ($<\omega_c$) is chosen then a normalised bandwidth will be $BW_n = BW/\omega_c$. New pole positions $s_{n1,2} = -\alpha_n \pm j\beta_n$ (where $\alpha_n = BW_n.\alpha$ and $\beta_n = BW_n.\beta$) exist for this BW_n, thus the new pole positions are $s_{n1,2} = BW_n.(-\alpha \pm j\beta)$. Figure 4.69 shows these pole transformed into the bandpass case with centre frequency ω_r normalised to 1 rad/sec.

Fig. 4.69 Normalised bandpass transformation.



BW_n = normalised −3dB bandwidth
ω_r = centre frequency normalised to 1 rad/sec

It can be seen that the radius of the circle upon which they lie has further contracted to $BW_n/2$ to give an overall bandpass bandwidth of BW_n. From the diagram the positions of all the poles (both $+\omega_r$ & $-\omega_r$) can be seen to be:

$$s_{1,2,3,4} = -\alpha\frac{BW_n}{2} \pm j\left(1 \pm \beta\frac{BW_n}{2}\right)$$

The poles of interest in the narrowband approximation are:

$$s_{1,2} = -\alpha\frac{BW_n}{2} + j\left(1 \pm \beta\frac{BW_n}{2}\right)$$

Using this equation the normalised pole positions from the origin i.e. the value of frequency for each bandpass section are given by:

$$\omega_{o1,2} = \sqrt{\left(\frac{\alpha BW_n}{2}\right)^2 + \left(1 \pm \frac{\beta BW_n}{2}\right)^2}$$

Where, as in the lowpass case, ω_o can be considered as a frequency scaling factor, this time to the normalised centre frequency ω_r. It is only necessary to calculate ω_{01} from the above equation, as the original transformation gives the more simple result $\omega_{o2} = 1/\omega_{o1}$ for a pole pair centred on ω_r.

The value of Q of each pole is also needed for the bandpass realisation and this calculated in the following manner:

By definition $Q = \frac{\omega_o}{BW}$ where ω_o and BW relate to a single pole normalised to 1 rad/sec in this case.

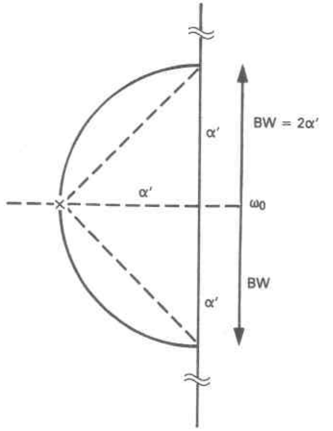
Figure 4.70 shows that for a single pole $BW = 2\alpha'$

Where $\alpha' = \alpha\frac{BW_n}{2}$; $\beta' = \beta\frac{BW_n}{2}$

From above $\omega_o = \sqrt{\alpha'^2 + (1 \pm \beta')^2}$

Thus $Q = \frac{\sqrt{\alpha'^2 + (1 + \beta')^2}}{2\alpha'}$;

Fig. 4.70 Q of a single pole.



For values of $BW_n < 0.2$ then $Q \simeq \frac{1}{2\alpha'}$

Odd orders of filter have a pole with $\beta' = 0$, $\omega_o = 1$ and $\alpha' = \alpha BW_n/2$ which is transformed from the negative real axis. For Butterworth filters the odd order pole always has a value of $\alpha = -1$. Values of α for odd order Bessel and Chebyshev filters are given in Tables 4.2(b) and 4.3 respectively.

For example a single pole filter with $f_r = 1\text{kHz}$ and $BW = 200\text{Hz}$ at -3dB would have a normalised bandwidth:

$$BW_n = \frac{BW}{\omega_r} = \frac{200}{1000} = 0.2$$

For a single pole $\alpha = -1$ and thus $\alpha' = \alpha\frac{BW_n}{2} = 0.1$

$$\therefore Q = \frac{1}{2\alpha'} = 5.$$

Thus the Q for an individual pole is obtained. (This can obtained directly from f_r/BW in this case, but this is not so for multipole filters.)

The attenuation at frequencies other than −3dB is given by manipulating the standard bandpass equation as follows:

$$H(s) = \frac{s\omega_r/Q}{s^2 + s\omega_r/Q + \omega_r^2};$$

Multiplying numerator and denominator by $Q/\omega_r s$ and substituting $s = j\omega$:

$$H(j\omega) = \frac{1}{1 + jQ\,(\omega/\omega_r - \omega_r/\omega)}$$

The attenuation in dB normalised to 1 rad/sec:

$$At_{dB} = -\,20\log\sqrt{1 + Q^2(\omega - 1/\omega)^2}$$

where $\omega - 1/\omega$ is the bandwidth $BW = \omega_U - \omega_L$ and $\omega_r = \sqrt{\omega_U\omega_L}$

Re-arranging gives $BW = \frac{\sqrt{At^2 - 1}}{Q}$

MFB Example

Using the MFB circuit of Figure 4.55(c) the transfer function given on page 4–49 is:

$$H(s) = \frac{-\,s(1/R_1C_1)}{s^2 + s(1/R_3)(1/C_1 + 1/C_2) + (1/R_3C_1C_2)(1/R_1 + 1/R_2)}$$

$$\omega_o/Q = (1/R_3)(1/C_1 + 1/C_2) \;\&\; \omega_o{}^2 = (1/R_3C_1C_2)(1/R_1 + 1/R_2)$$

Where ω_o is the normalised values of ω_r.
make $C_1 = C_2 = C$

$$\therefore\ R_3 = \frac{2Q}{\omega_oC} \text{ and } \omega_o{}^2 = \frac{1}{C^2\,R_3\,R}; \quad \text{where } \frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2}$$

$R = \frac{1}{2Q\omega_oC}$ by substitution of R_3 and re-arranging.

Thus as $\omega_o = 1$ for single pole $R_3 = \frac{2Q}{C}$ & $R = \frac{1}{2QC} = \frac{R_3}{4Q^2}$

Choose C = 10nF and scaling for centre frequency ω_r

$$R_3 = \frac{2Q}{\omega_rC} = \frac{10}{2\pi\times 10^3 \times 10^{-8}} = 159.15 \text{ kohm (160k)}$$

$R = R_3/100 = 1.6$ kohm.

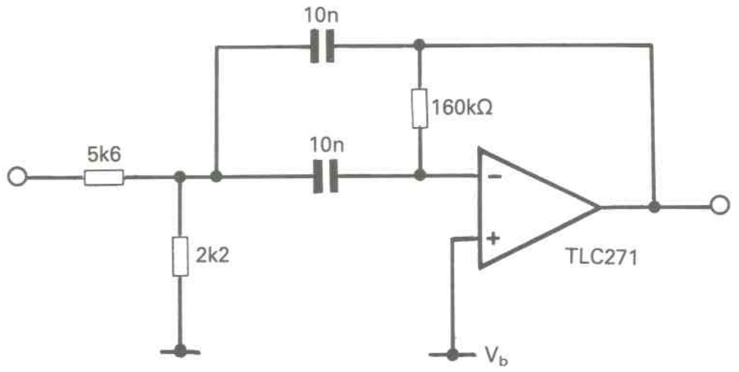
The circuit implemented using a TLC271 is shown in Figure 4.71.

Circuit gain: at $\omega = \omega_r$: $H_r = \frac{-(1/R_1C)}{(2/R_3C)} = -\frac{R_3}{2R_1}$

Substituting for R_3 and C: $H_r = -\,2Q^2\frac{R_2}{R_1 + R_2} = 13.92$

From the requirement that the op-amp open loop gain is 10 times the circuit closed loop gain, a gain of >140 is needed. This sets the highest frequency at which this circuit, with the values shown, can operate. From Figure 3.16 this is approximately 20kHz for high bias mode TLC27_ LinCMOS op-amps.

Fig. 4.71 MFB bandpass filter fr = 1KHz Q = 5.



When tuning the circuit for frequency the ratio of R_3 to R should be kept constant to maintain the same Q value.

Chebyshev 3 pole State Variable Filter Example

Taking as an illustrative example a filter specification of: Centre frequency $f_r = 5$kHz, −3dB bandwidth = 500 Hz, −40dB bandwidth = 2kHz and <1.5dB ripple, the circuit values for a State Variable circuit are calculated as follows:

$$\text{Shape factor } H_s = \frac{\text{Bandwidth at required attenuation}}{-3\text{dB Bandwidth}} = \frac{BW_x}{BW_3}$$

$$= \frac{2000}{500} = 4$$

With reference to Figure 4.48(b) a 3 pole filter with $\omega/\omega_c = 3.5$ and 1dB ripple meets the requirement.

Table 4.3 gives the pole positions as: $s_1 = -0.4513$,
$s_{2,3} = -0.2257 \pm j0.8822$.

using $\alpha' = \alpha BW_n/2$ & $\beta' = \beta BW_n/2$
$BW_n = 500/5000 = 0.1$
$\alpha'_1 = 0.002256 \quad \therefore\ Q_1 = \frac{1}{2\alpha_1'} = 22.15$
$\omega_o = \sqrt{\alpha'^2 + (1 + \beta')^2}$

Giving $\omega_{o2} = 1.0412$ and $\omega_{o3} = 1/\omega_{o2} = 0.9605$ and $Q_{2,3} = 44.3$

Using the transfer function for the State Variable Filter of page 4–51 and circuit of figure 4.56(b) the values of Q and ω_r can be found in terms of component values.

$$H(s) = \frac{-K \times s(1/R_1C_1)}{s^2 + s(Rq/R)(1/R_1C_1) + (1/R_1C_1)^2}$$

Then $\omega_r = \frac{1}{R_1C_1}$ and $\frac{\omega_r}{Q} = \left(\frac{Rq}{R}\right) \times \left(\frac{1}{R_1C_1}\right) \quad \therefore\ Q = \frac{R}{R_q}$

and thus Q and ω_r are independently adjustable.

First section with $f_r = 5$kHz and $Q = 22.15$

Choose $C_1 = 2.2$nF then $R_1 = \frac{1}{2\pi \times 5 \times 10^3 \times 2.2 \times 10^{-9}} = 14.47$ kohm

Choose R = 100k then $R_q = 100/22.15 = 4.515$ kohm

Second section: $C_1 = 2.2$nF, $R_1 = 15.06$ kohm, $R_q = 2.257$ kohm.

Third section: $C_1 = 2.2$nF, $R_1 = 13.89$ kohm, $R_q = 2.257$ kohm.

In practice when the circuit is constructed an adjustment of values may be required to allow for layout and op-amp performance. These are seen as shifts in pole frequencies and Q enhancement from the calculated values. As higher values of Q are used there will be greater the sensitivity to component tolerances. The gain of the State Variable Filter circuit is found by substituting $s = 1/R_1C_1$ in the transfer function above and gives a filter gain of KQ. An op-amp open loop gain of at least 3Q is required at the frequency of operation. The levels of input signal that can be handled are limited by the dynamic range (supply voltage and noise) and the slew rate. Using values of K less than unity

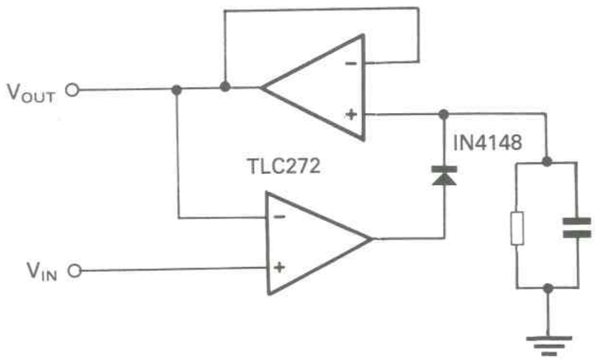
allows higher input signal amplitudes to be filtered, but does not improve the dynamic range.

This filter can be implemented using LinCMOS TLC274 high bias mode quad op-amps, and thereby utilises their larger gain-bandwidth and slew rate.

5. Application Circuit Memory Joggers

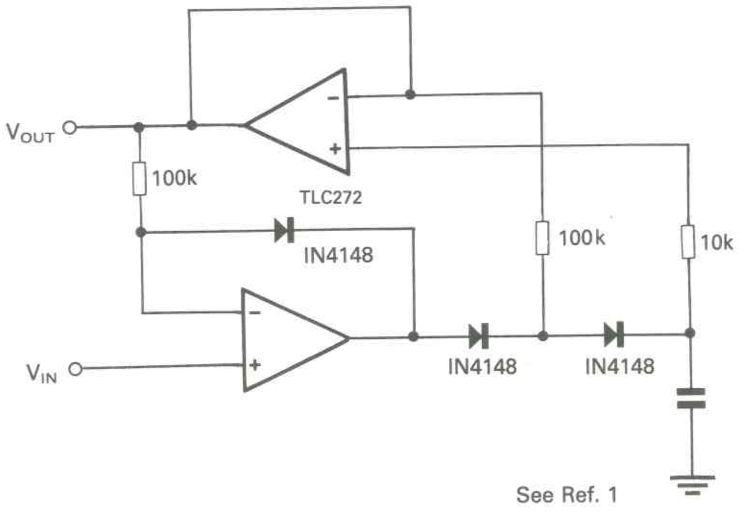
SAMPLING CIRCUITS

Fig. 5.1 Peak detector.



See Ref. 1

Fig. 5.2 Low drift peak detector.



See Ref. 1

Fig. 5.3 Basic sample and hold.

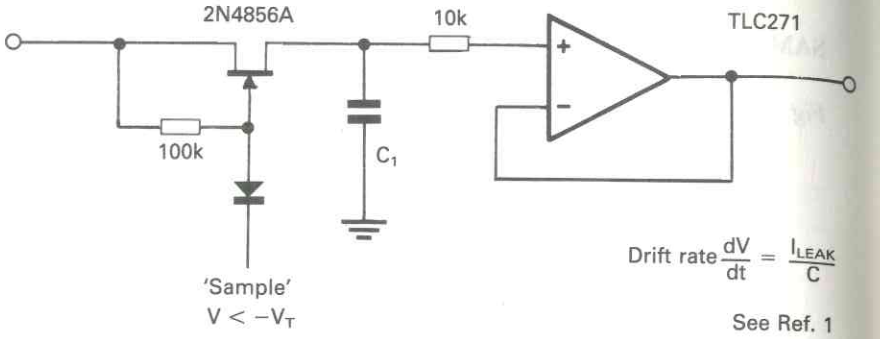


Fig. 5.4 Low drift sample and hold.

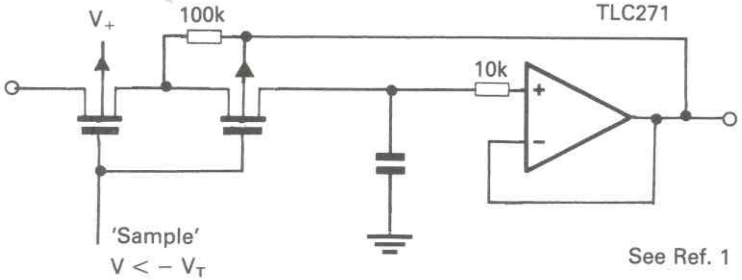


Fig. 5.5 High accuracy sample and hold.

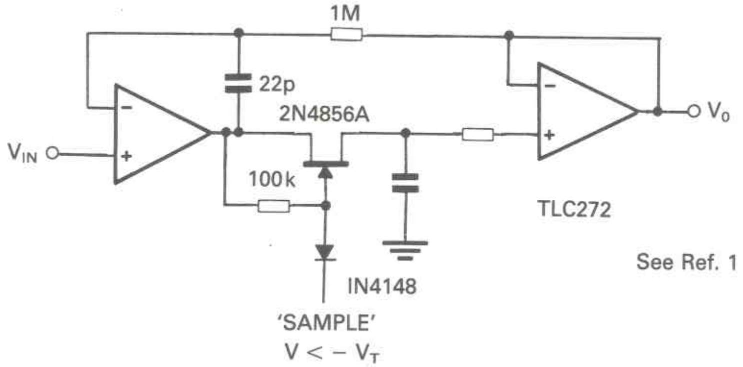
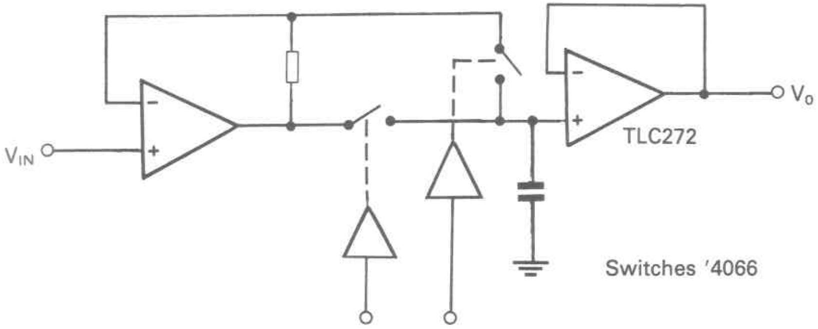


Fig. 5.6 Fast sample and hold.



RECTIFIERS

Fig. 5.7 Precision full wave rectifier (absolute value circuit).

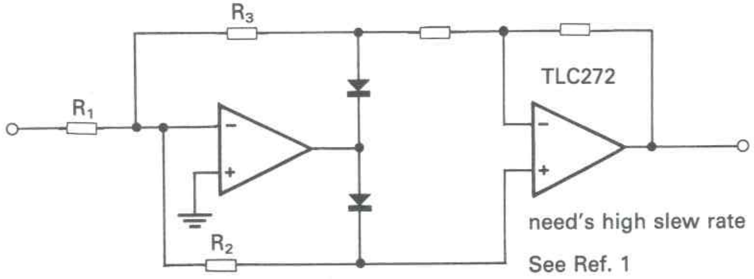
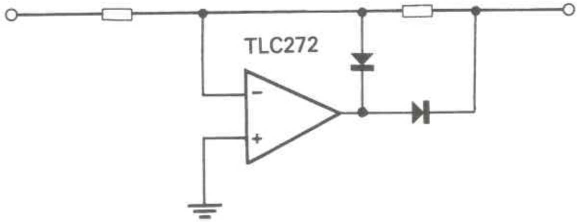
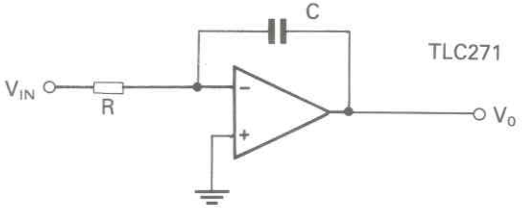


Fig. 5.8 Halfwave rectifier.



INTEGRATOR CIRCUITS

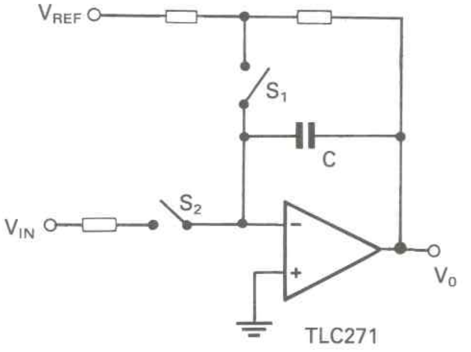
Fig. 5.9 Basic integrator.



$$V = -\frac{1}{RC}\int V_{IN}dt + \underbrace{\frac{1}{RC}\int V_{IO}dt + \frac{1}{C}\int I_{IB}dt + V_{IO}}_{\text{error terms}}$$

See Ref. 1

Fig. 5.10 Three mode integrator.

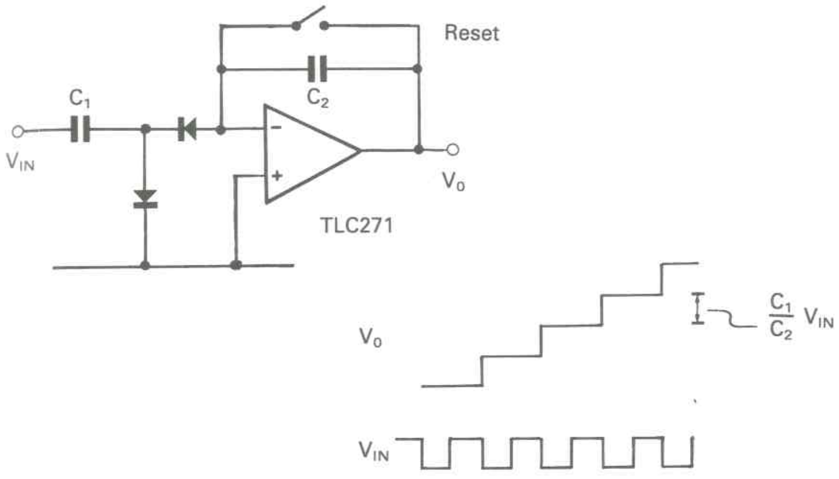


	S_1	S_2
Reset	1	0
Integrate	0	1
Hold	0	0

S_1 & S_2 4066

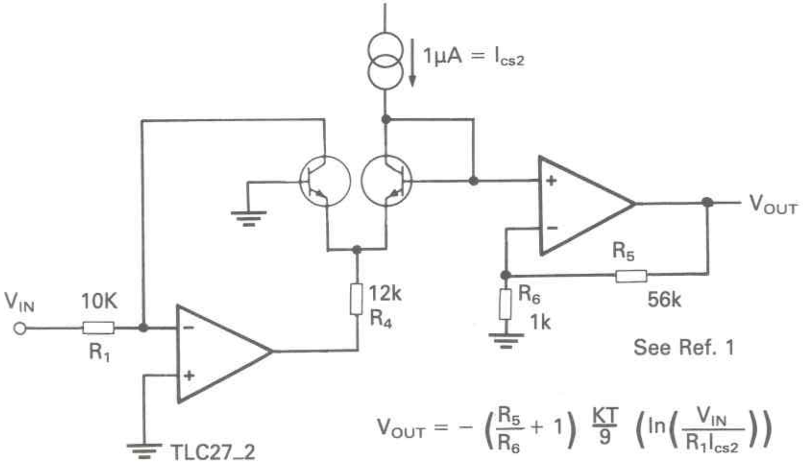
performance limited by slew rate and output current to charge C.

Fig. 5.11 Linear staircase generator.



AMPLIFIER CIRCUITS – LOG – PHOTO – DIODE ETC.

Fig. 5.12 Logarithmic amplifier.



See Ref. 1

$$V_{OUT} = -\left(\frac{R_5}{R_6} + 1\right)\frac{KT}{q}\left(\ln\left(\frac{V_{IN}}{R_1 I_{cs2}}\right)\right)$$

Fig. 5.13 Photo diode amplifier with ambient light rejection.

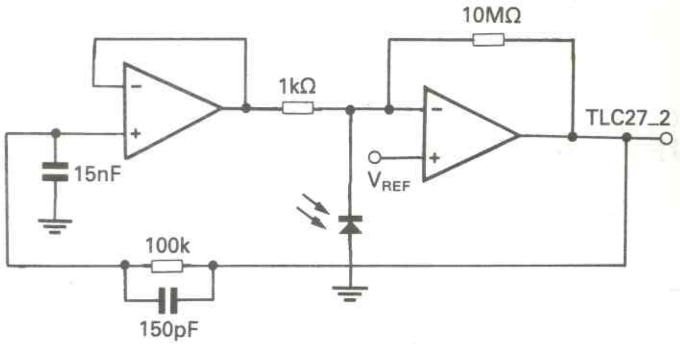


Fig. 5.14 Null detector.

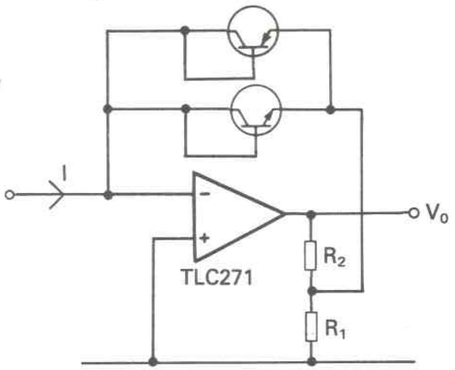


Fig. 5.15 Basic A.C. millivoltmeter.

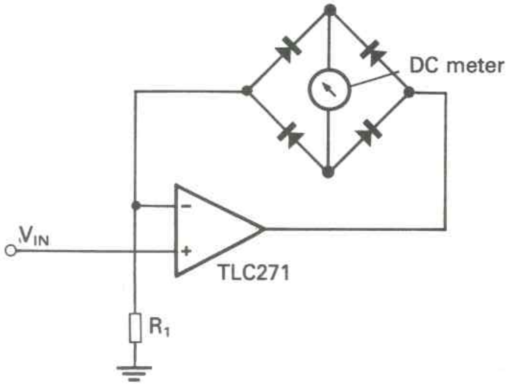
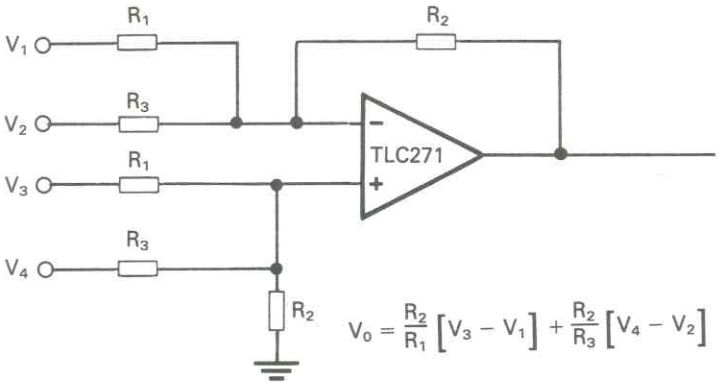
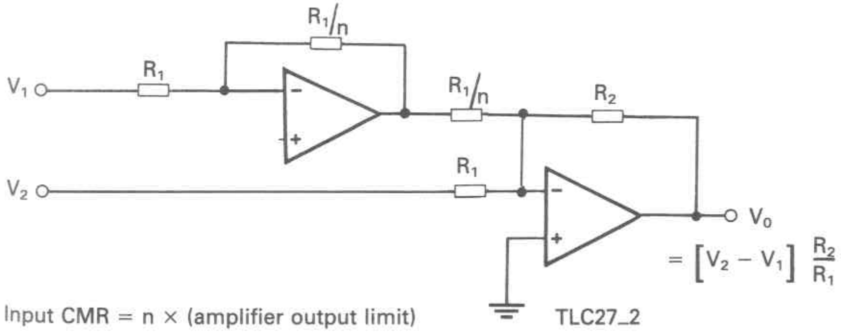


Fig. 5.16 Adder subtractor.



$$V_o = \frac{R_2}{R_1}\left[V_3 - V_1\right] + \frac{R_2}{R_3}\left[V_4 - V_2\right]$$

Fig. 5.17 Differential amp with high common mode rejection.



$$= \left[V_2 - V_1\right] \frac{R_2}{R_1}$$

Input CMR = n × (amplifier output limit)

FUNCTION CIRCUITS

Fig. 5.18 Frequency voltage converter.

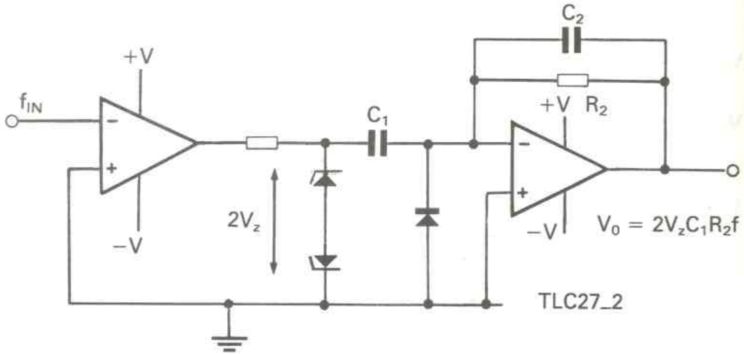
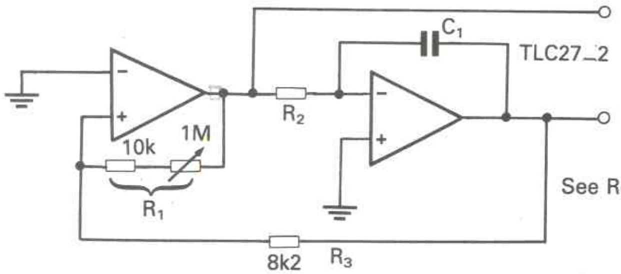


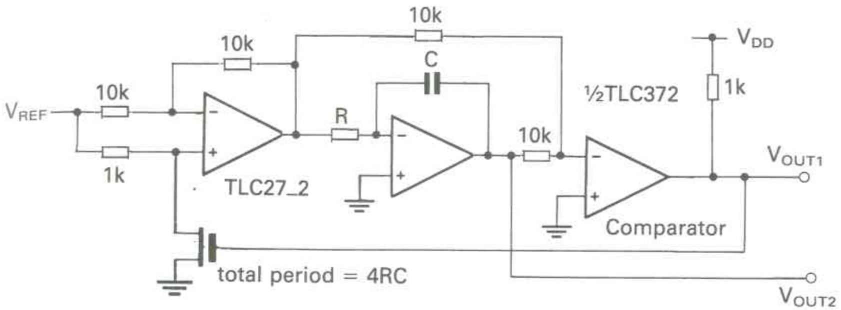
Fig. 5.19 Basic triangle/squarewave generator.



See Ref. 1

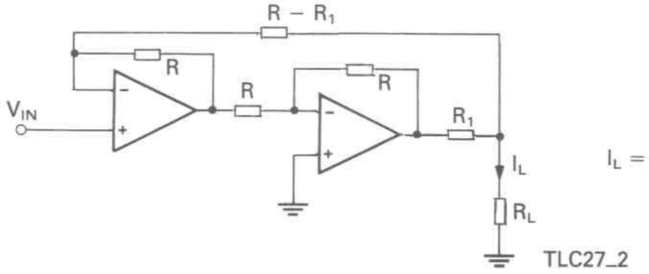
$f_{osc} = \frac{R_1}{4C_1R_2R_3}$ Integrator error $\left[\pm \frac{V_{IO}}{CR} + \frac{I_{IB}}{C}\right]$ Causes asymmetry at low frequencies, this is minimised by low I_{IB} LinCMOS & V_{IO} selections.

Fig. 5.20 Variable amplitude triangle generator.



See Ref. 1

Fig. 5.21 Voltage to current converter.



$I_L = \frac{2V_{IN}}{R_1}$

Fig. 5.22 Pulse width modulator.

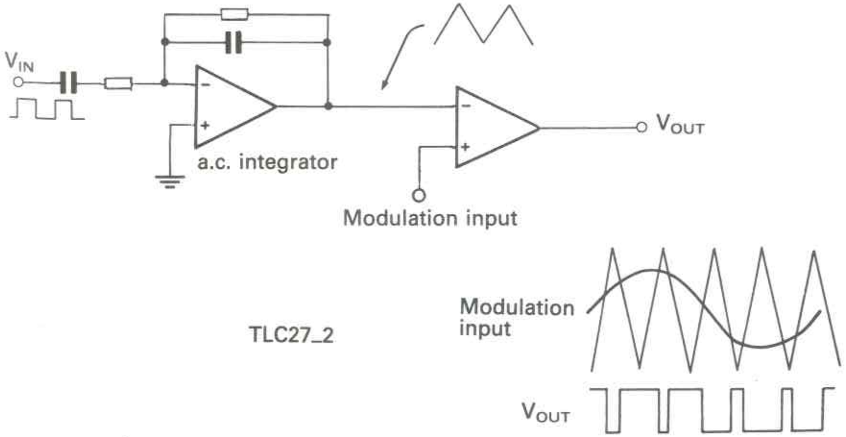
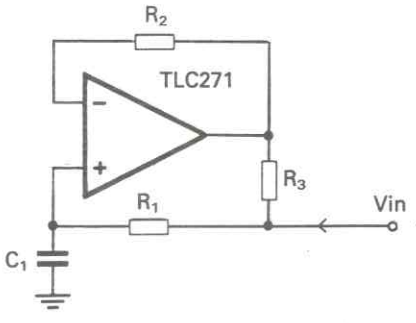


Fig. 5.23 Capacitance multiplier

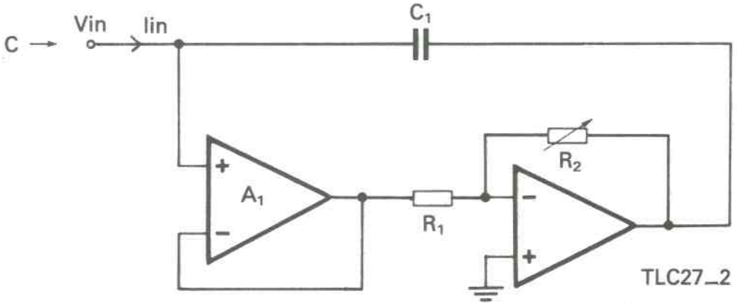


$R_1 = R_2$

$\leftarrow C' = C_1 \left[\frac{R_1 + R_3}{R_3}\right]$

See Ref 1

Fig. 5.24 Variable Capacitance Multiplier

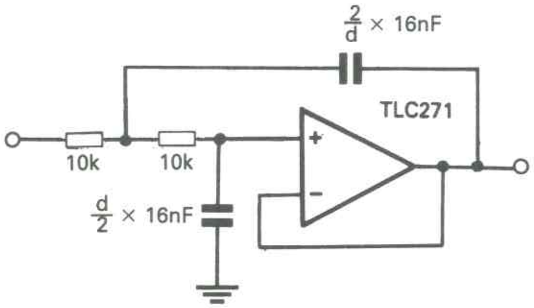


$C' = C_1 \times \left[\frac{R_2}{R_1} + 1\right]$

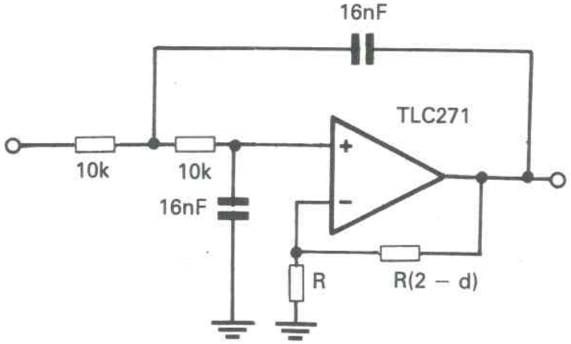
See Ref 1

FILTERS

Fig. 5.25 Lowpass VCVS.



Unity gain Sallen & Key (VCVS) normalised to: f_c = 1kHz Z = 10k ohms.



Equal component Sallen & Key, gain = +(3 − d), normalised to: f_c = 1kHz
Z = 10k ohms.

Fig. 5.26 Lowpass MFB.

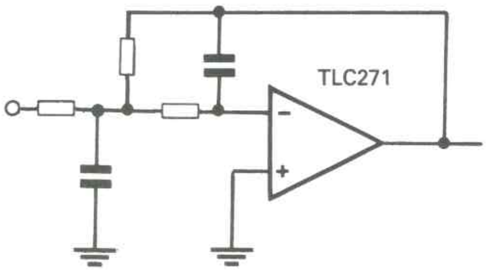
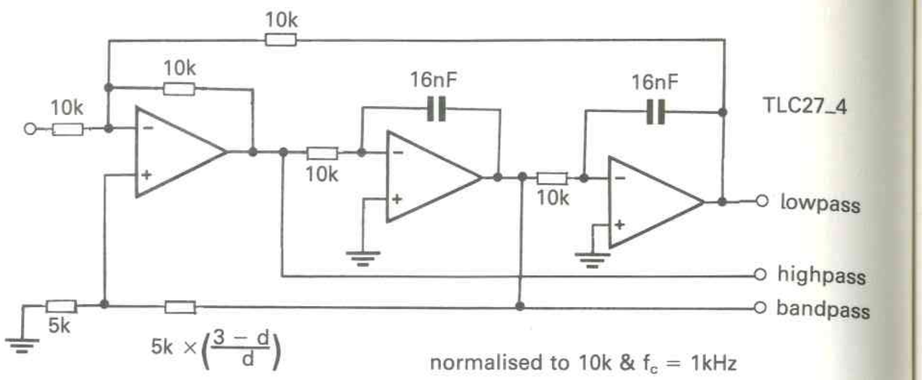
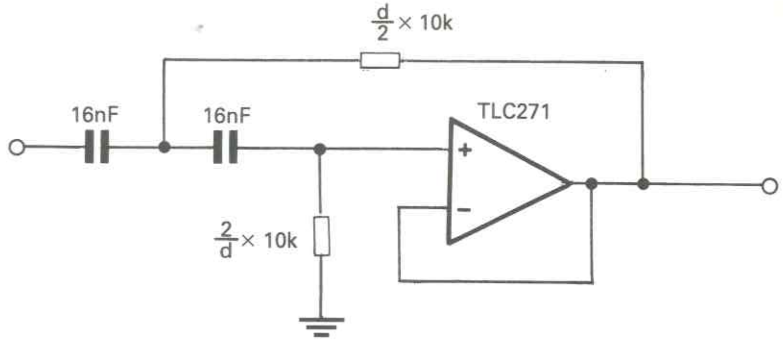


Fig. 5.27 State variable.

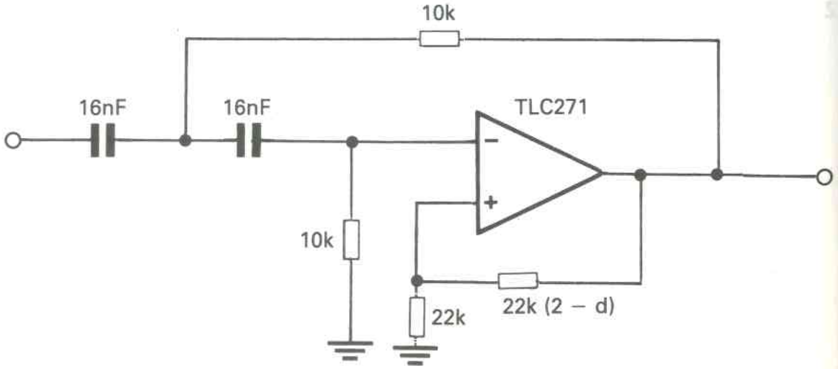


normalised to 10k & $f_c = 1\text{kHz}$

Fig. 5.28 High pass VCVS.

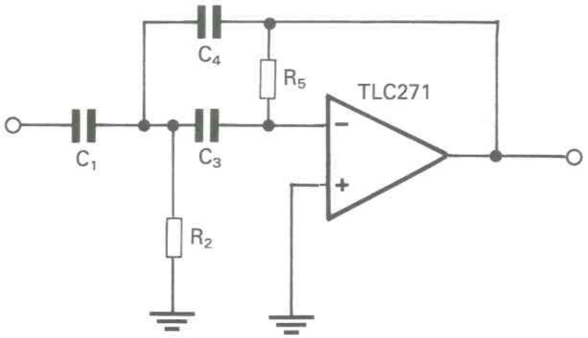


Unity gain VCVS normalised to 1kHz at 10k ohm



Equal component VCVS gain = + (3 − d) normalised to 10kHz $f_i = 1\text{kHz}$

Fig. 5.29 Highpass MFB.



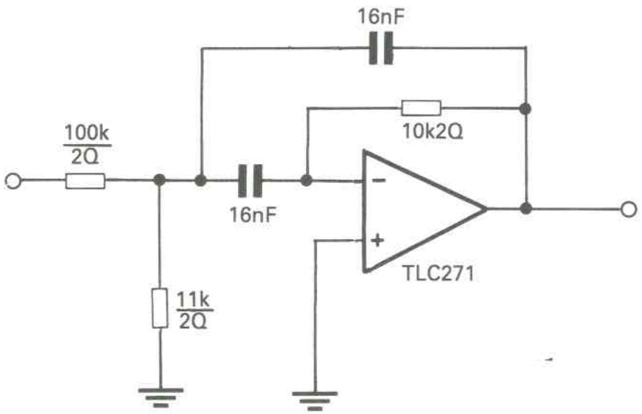
MFB high pass: given gain $H_0.d$, ω_0, put $C = C_1 = C_3$

$$R_5 = \frac{1}{d\omega_0 C}(2H_0 + 1),$$

$$R_2 = \frac{d}{\omega_0 C\,(2H_0 + 1)},$$

$$C_4 = \frac{C_1}{H_0}$$

Fig. 5.30 Bandpass MFB.



Normalised to 10k/ at $f_c = 1\text{kHz}$, $Q < 5$.

Fig. 5.31 Biquad.

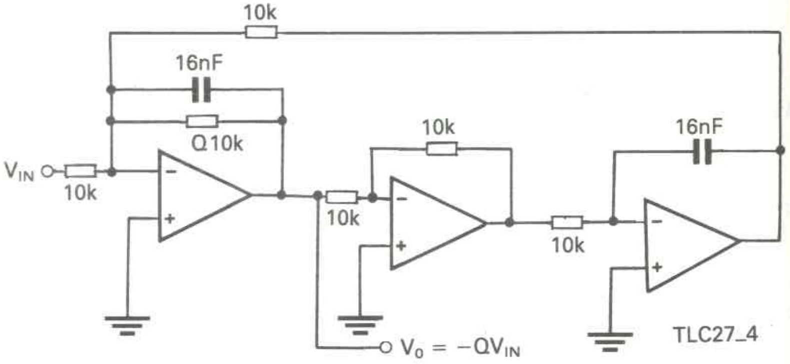
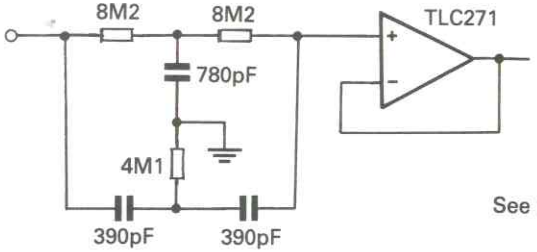
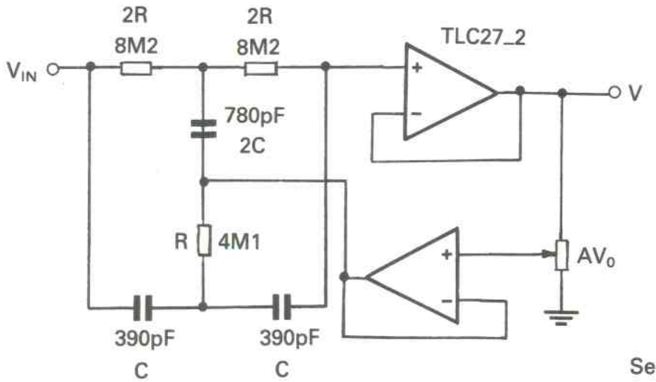


Fig. 5.32 Twin T 50Hz notch filter.



See Ref. 1

Fig. 5.33 Adjustable Q notch filter.



See Ref. 1

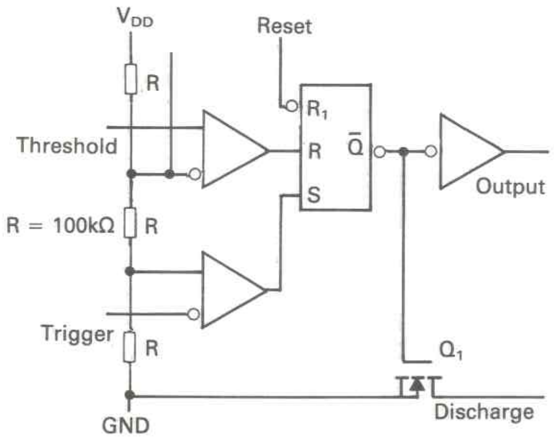
$$\frac{V_o}{V_{IN}} = \frac{4s^2R^2C^2 + 1}{4s^2R^2C^2 + (1 - A)\,8sRC + 1}$$

6. LinCMOS Timers

DESCRIPTION

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS process. Due to its high-impedance inputs (typically $10^{12}\Omega$), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors than the NE555. Like the NE555, the TLC555 achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The LinCMOS process allows the TLC555 to operate at frequencies up to 2MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 1 mW at V_{DD} = 5 V) over a wide range of supply voltages ranging from 2 volts to 18 volts.

Fig. 6.1 Functional block diagram.



1. Reset can override Trigger, which can override Threshold.
2. All unused inputs should be tied to an appropriate logic level to prevent false triggering.

Like the NE555, the threshold and trigger levels are normally two-thirds and one-third respectively of V_{DD}. These levels can be